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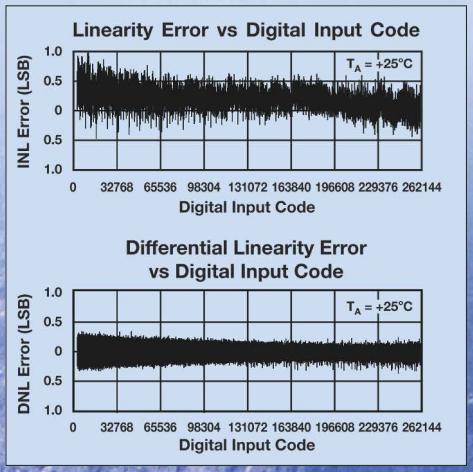

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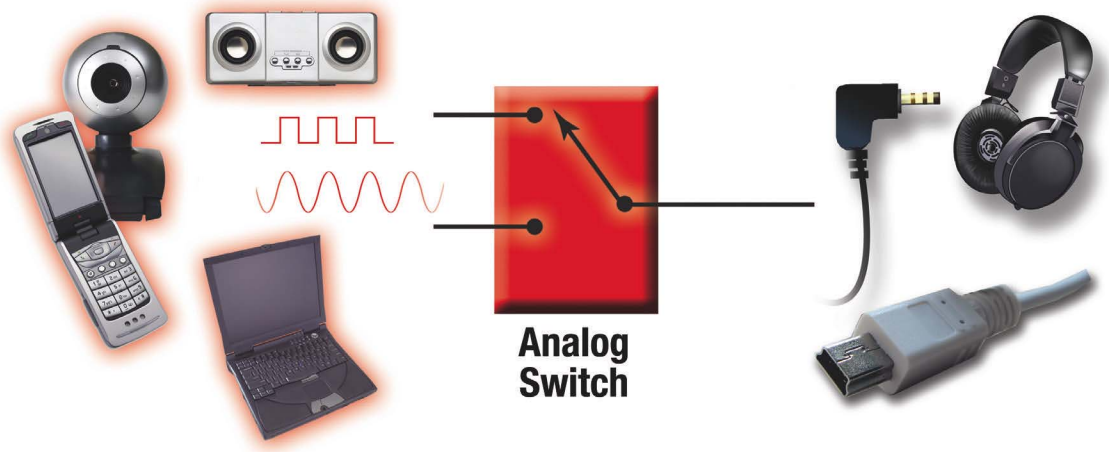

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TS5A23166	SPST x 2	0.9	0.25	0.1	1.65	5.5	2 kV HBM	7.5	11	US8-8, WCSP-8
TS3A4751	SPST x 4	0.9	0.4	0.05	1.65	3.6	4 kV HBM	14	9	TSSOP-14, **SON-14, µQFN-14**
TS5A6542	SPDT	0.75	0.25	0.25	2.25	5.5	15 kV Contact (IEC L-4)	25	20	WCSP-8, µQFN-8
TS5A3159A	SPDT	0.9	0.25	0.1	1.65	5.5	2 kV HBM	30	20	SC70-6, SOT23-6, WCSP-6
TS5A12301E	SPDT	0.75	0.1	0.1	2.25	5.5	8 kV Contact (IEC L-4)	225	215	WCSP-6
TS5A23159	SPDT x 2	0.9	0.25	0.1	1.65	5.5	2 kV HBM	13	8	MSOP-10, QFN-10
TS3A24159	SPDT x 2	0.3	0.04	0.05	1.65	3.6	2 kV HBM	35	25	WCSP-10, SON-10, VSSOP-10
TS5A26542	SPDT x 2	0.75	0.25	0.25	2.25	5.5	15 kV Contact (IEC L-4)	25	20	WCSP-12
TS5A22362/4	SPDT x 2	0.94	0.46	0.11	2.3	5.5	2.5 kV HBM	80	70	WCSP-12, SON-10, VSSOP-10
TS3USB221	SPDT x 2	6	1	0.2	2.3	3.6	2 kV HBM	30	12	SON-10, µQFN-10
TS3A44159	SPDT x 4	0.45	0.1	0.07	1.65	4.3	2 kV HBM	23	32	TSSOP-16, SON-16, µQFN-16
TS5A3359	SP3T	0.9	0.25	0.1	1.65	5.5	2 kV HBM	21	10.5	US8-8, WCSP-8
TS3A5017	SP4T x 2	12	9	2	2.3	3.6	2 kV HBM	9.5	3.5	TVSOP-16, SON-16, **µQFN-16**

Red text denotes new products and new package addition

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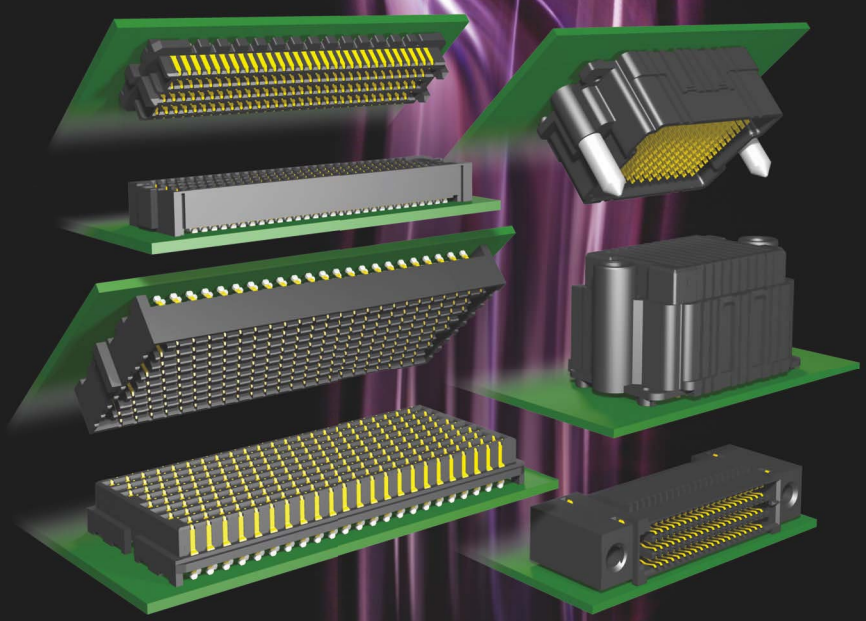

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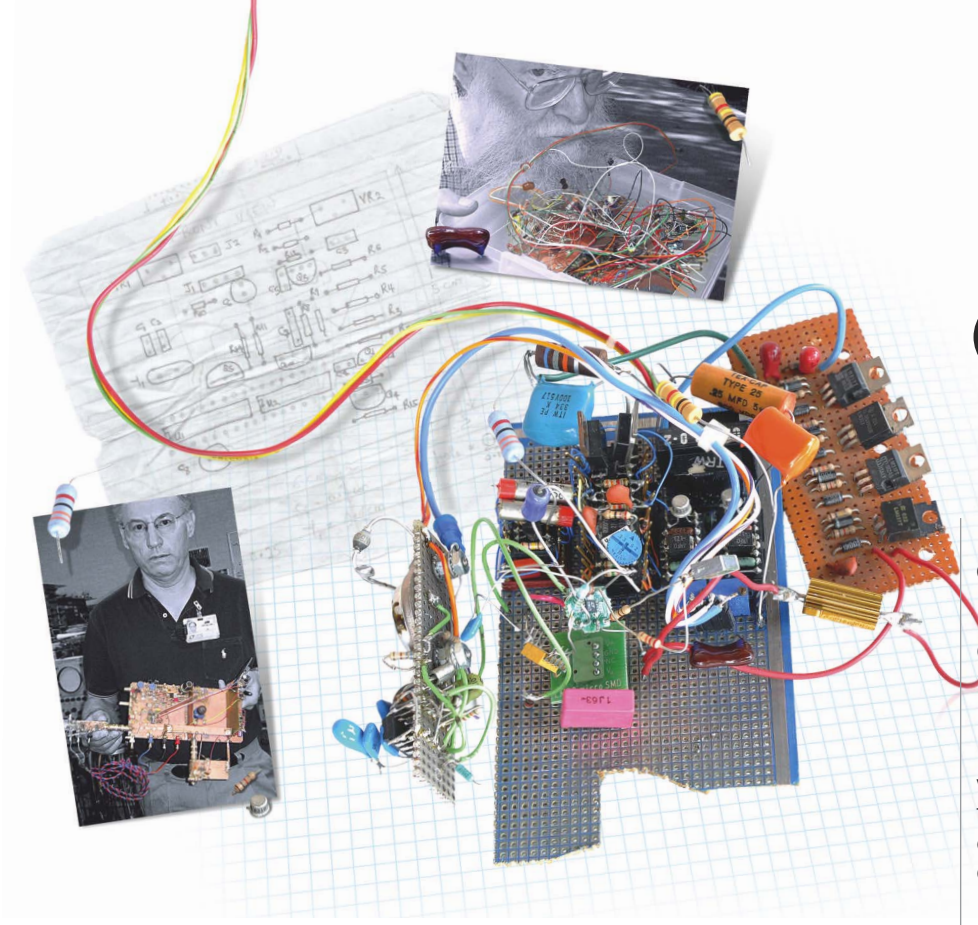

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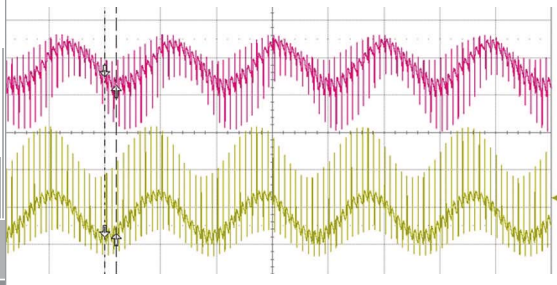

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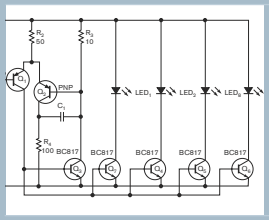

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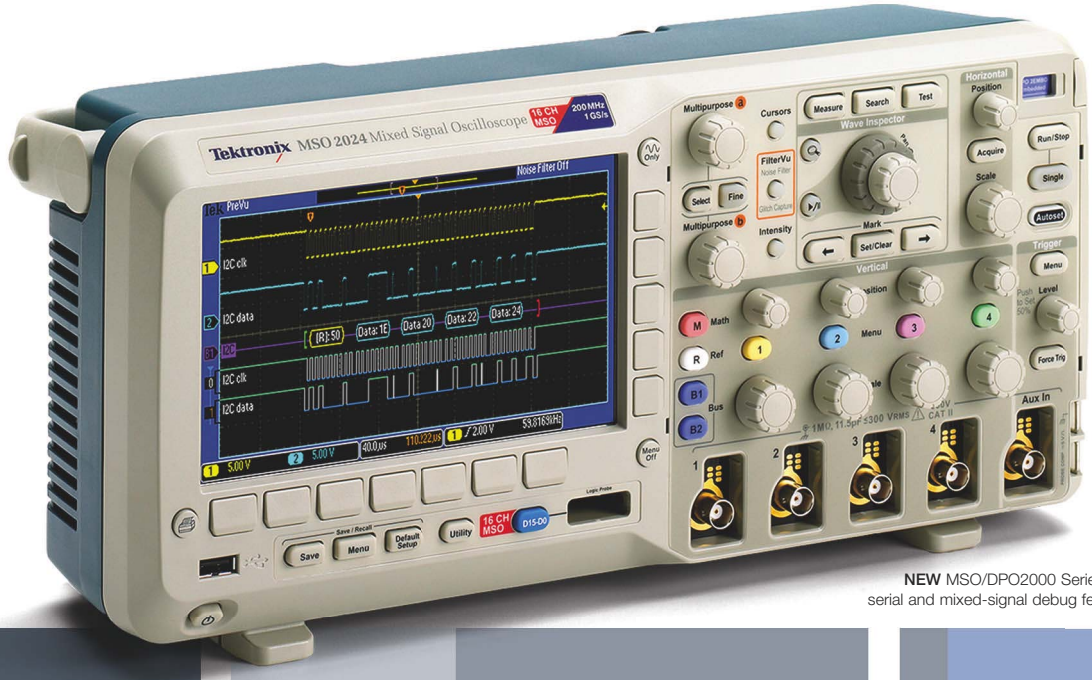

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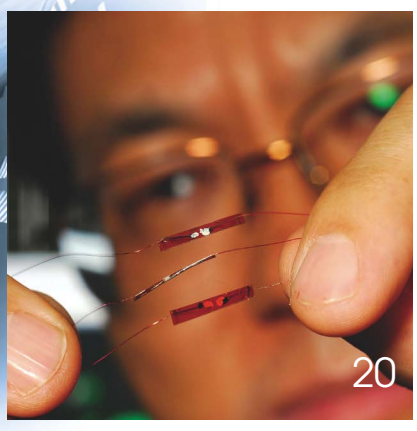

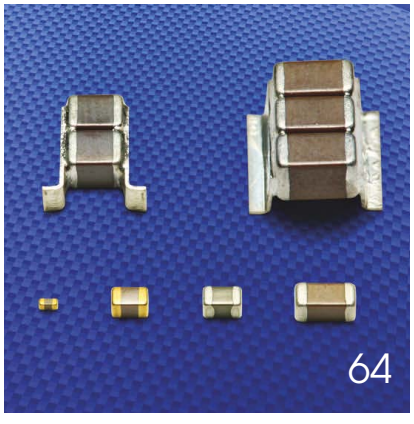

DEPARTMENTS & COLUMNS

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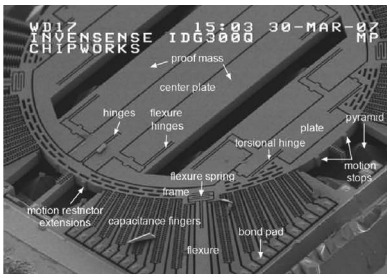

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THIS WEEK IN GEEK

EDN's Friday tech roundup, available in the *Now Hear This* blog.
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BY BRIAN DIPERT, SENIOR TECHNICAL EDITOR

Bias and opinion in tech and in life

I recently received a fairly critical e-mail that began with an eye-catching and eyebrow-raising subject line: "Bait and switch?" The reader who sent the e-mail appeared to be quite disappointed because of my recent cover story (**Reference 1**). In the article, I wrote about virtualization instead of covering hardware—specifically, CPU-instruction-set—emulation, which is the topic he was interested in. He was frustrated despite the fact that my article's title began with the word *virtualization*, not *emulation*.

To be fair, the first draft of the article included a sidebar in which I'd explicitly directed readers to the *Brian's Brain* blog, where they'd find a post on emulation, among others. The sidebar was cut at the last minute due to limited available space. Perhaps, had the sidebar survived the editing process and had he seen it, the reader would have been less disappointed. Then again, he admitted that he didn't make it past the first paragraph of my article.

As I shook my head with bemusement and other emotions at this reader's narrowly focused agenda, I thought back to one of the top sessions I attended in October at the Audio Engineering Society Convention. The panel session, titled "Engineering Mistakes We Have Made in Audio," featured several well-known hardware and software technical experts.

I was gratified to see that many of the topics the panelists talked about were psychological in nature; that is, they were reflective of the tendency to enter into definition, design, and debugging situations with predetermined and rigid ideas of the end result. For example, there was the situation in which the computer hard drive failed and the presenter sequentially popped in—and ruined—*all* of the backup tapes before he discerned that the tape drive, not the tapes, had also gone bad. Similarly, another presenter fried an entire set of add-in cards by not realizing, until it was too late, that the backplane-connector hookup, not the add-in card design, was at fault.

I realize that my approach can't be completely distortion-free, which is why I'm an advocate of network neutrality.

I encounter examples of narrow, rigid perspectives and predetermined conclusions all the time in the feedback I receive to my online and print write-ups. Vudu-set-top-box owners, desperate to justify their investments, ignore the hard data that indicates that the company is making inappropriate use of their LAN and WAN bandwidth for its own benefit. Back in the days of the HD-DVD-versus-Blu-ray-format war, equipment and content owners in each camp similarly fought with me and with each other, angry that I wouldn't agree that their wallet-anointed preference was all-good—and the opposing camp's option was all-bad. Apple and Linux backers think I'm a Microsoft mouthpiece. AMD and Nvidia fans respond the same way whenever I say anything remotely positive about Intel. Nobody, it seems, roots for the market leader.

However, I need to remain diligent regarding the possibility of narrow, rigid perspectives and predetermined conclusions creeping into *my* psyche, too. Unlike some other journalists, I don't believe that being balanced means presenting an exactly equivalent number of pros and cons for each side of an issue. I do the research, in as undistorted a fashion as I can muster, and then I present the data and my conclusion. Because I'm a human being, not a computer or, for that matter, a Vulcan, I realize that my approach can't be completely distortion-free, which is why I'm an advocate of network neutrality—enabling access to a diversity of perspectives by a thereby-informed populace. But what I *can* commit to is flexibility; as new data emerges, I strive to revisit and, if necessary, alter my previous conclusions.

I welcome your thoughts, either tech-specific or more general. EDN

REFERENCE

1 Dipert, Brian, "Virtualization: silicon and software salvation or technological tower of Babel?" *EDN*, Oct 2, 2008, pg 34, www.edn.com/article/CA6598366.

Contact me at bdipert@edn.com.

Go to www.edn.com/081205eda for a more in-depth discussion of these topics.

Read a follow-up blog post at www.edn.com/081205edb.

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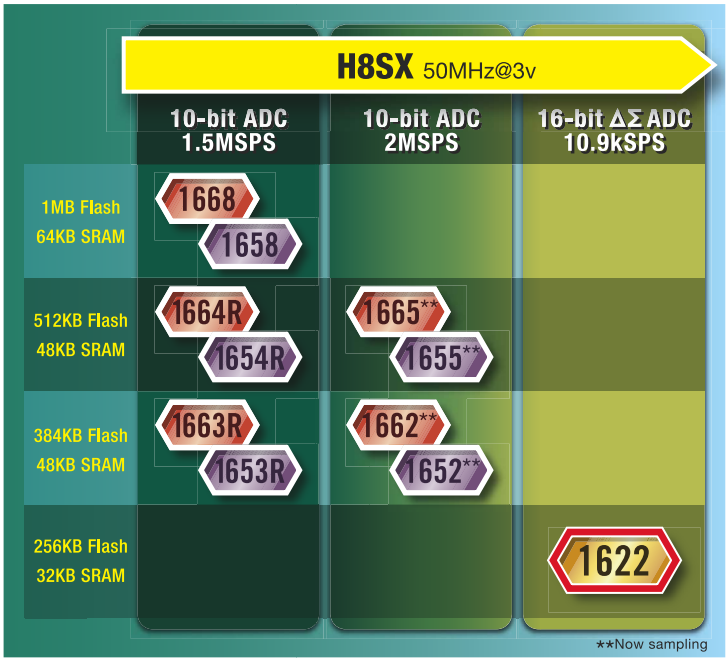

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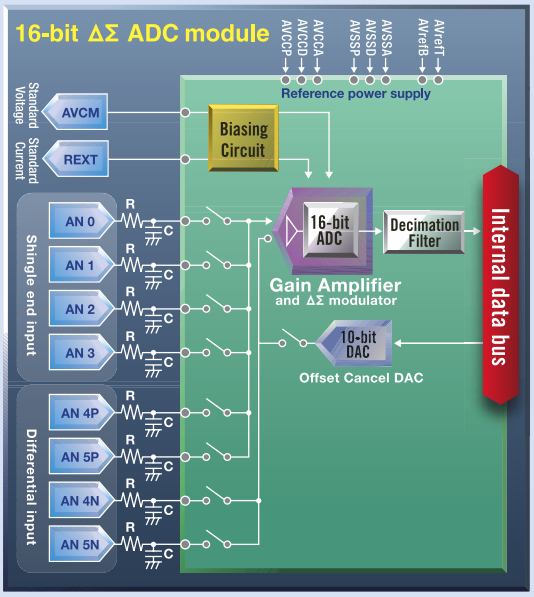

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*Source: Gartner "Semiconductor Applications Worldwide Annual Market Share: Database" Hiroyuki Shimizu, 27 March 2008, GJ08218 ＊This is 2007 ranking

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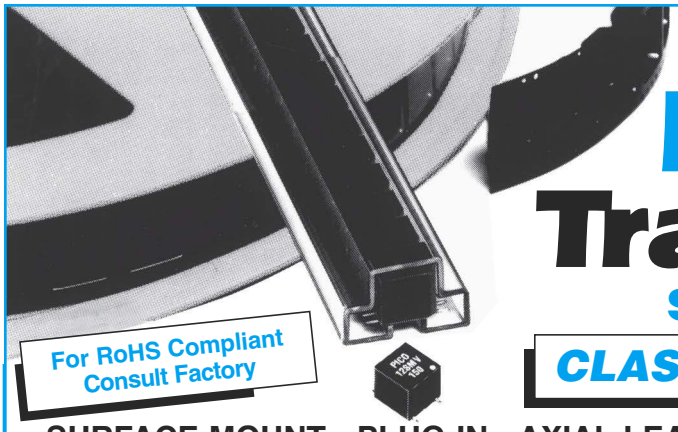

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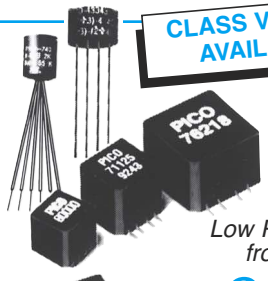

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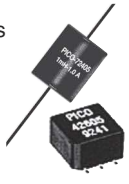

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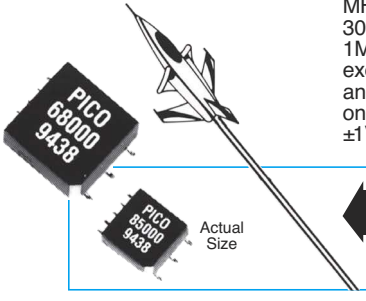

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Surface Mount **electrical equivalents of QPL-MIL-PRF-21038/27**

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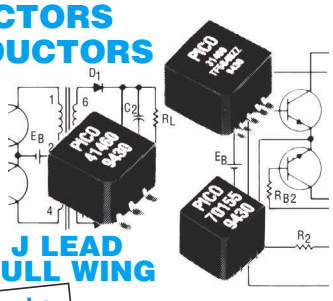

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INNOVATIONS & INNOVATORS

Power-stingy digital accelerometers yield benefits in gesture-driven consumer devices

Features involving a device's motion, such as a tap-to-mute capability on a cell phone or a user-input feature on a gaming controller, can serve as communication tools. Motion sensors can also serve as safety devices, sensing a laptop in a freefall dive and shutting down the hard drive. It's difficult to use one accelerometer for all these functions because different sensing applications require different g-force ranges. For example, freefall detection requires about 1.5g, a handheld motion-detection system for gaming control requires about 3g, and low-vibration monitoring for shipping applications requires 4 to 6g. Few consumer products can support the cost of either a multiple-accelerometer implementation or a one-expensive-device implementation that can support the entire range.

To address this problem, Freescale's new three-axis MMA745xL digital accelerometer offers a selectable range of sensitivity that covers 2, 4, and 8g; changing between sensitivities requires only about 5 msec. The device communicates with its supervisory processor over either an I^2C (inter-integrated-circuit) or an SPI (serial-peripheral-interface) bus. The sensor's sensitivity is 64 LSB/g at 2 or 8g in 10-bit mode. The sensor has miserly power needs of 400 µA in its normal operation and just 5 µA in sleep mode. The typical wait time after initial power-up is 1 msec, and the maximum response time to awaken from sleep mode is 20 msec. The device's power voltage can range from 2.4 to 3.6V, and I/O pins are 1.8V-compatible. It comes in a 14-pin, 3×5×1-mm LGA package and has an operating-temperature range of −40 to +85°C.

Freescale offers the ZSTAR 3 (ZigBee sensing triple-axis reference design 3) to speed development of MMA745xL wireless-system applications, such as motion dialing in cell phones, antitheft detection for laptops, and motion sensing for pedometers. The ZSTAR3 kit accommodates multiple digital and analog accelerometer boards, which connect through a 2.4-GHz RF ZigBee communication interface to a PC's USB port. The board's microcontroller-I/O pins power the MMA745xL, which requires less than 500 µA. The board consumes less than 1 µA in sleep mode because it turns the sensor completely off, rather than using the sensor's sleep mode. The ZSTAR3 transmits at 30 samples/sec. To conserve power, the ZSTAR3 software skips transmission if the sensor output data is the same as or similar to the last transmitted sample. Prices for the MMA745xL sensor start at $2.60 (10,000), and the ZSTAR3 reference platform sells for $99 (one).**—by Margery Conner**

▷**Freescale**, www.freescale.com.

FEEDBACK LOOP

"All that 'free' spectrum is sure tempting, but let's work the bugs out of DTV before the FCC lets the cows out of the barn because we all know that, once they're out, you're never gonna get 'em back."

—Reader and electrical engineer Jonathan Williams, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6602449. Add your comments.

The three-axis MMA745xL digital accelerometer offers a selectable range of sensitivity that covers 2, 4, and 8g to enable gesture-driven communication in consumer devices, such as cell phones.

Scalable instrument ups speed, accuracy of MIMO-receiver lab tests

Agilent Technologies has announced a scalable laboratory instrument that enables quicker, more accurate testing of MIMO (multiple-input/multiple-output) receivers earlier in the design cycle. Providing what the company calls the market's best simulation of real-world conditions, the new N5106A PXB MIMO-receiver tester enables significant reductions in the time required to develop and qualify new products.

By minimizing design uncertainty and setup time and providing the performance and scalability to meet future test needs, the instrument transforms MIMO test, according to Agilent. Its capabilities make the new tester ideal for R&D engineers who develop and integrate MIMO receivers for 3GPP (third-generation-partnership-project), LTE (long-term-evolution), WiMax (worldwide-interoperability-for-microwave-access), and emerging wireless standards.

The tester provides versatile signal creation and channel emulation for the latest LTE and WiMax standards. It supports 2×2 (two-transmitter/two-receiver), 2×4 (two-transmitter/four-receiver), and 4×2 (four-transmitter/two-receiver) MIMO with 120-MHz bandwidth and features custom MIMO-correlation settings—for example, channel models, antenna pattern, and correlation matrix. Signal Studio signal-creation software runs in the instrument and provides up-to-date, standards-compliant signal creation.

> Adding support for the test needs of future technologies requires only a cost-effective upgrade that you can perform in an hour.

Behind its simple front panel, the PXB MIMO-receiver tester incorporates scalable hardware and Windows-based software that can make short work of what—until now—has been an extremely complicated testing problem.

Using the PXB, you can simulate real-world conditions in the lab to more quickly test corner cases and stress devices beyond standards requirements. You can also test coexistence to ensure design robustness earlier in the design process. Using Signal Studio, Advanced Design System software, or even a waveform-creation tool that you wrote yourself, you can sum the outputs of as many as four high-performance baseband generators to perform multiformat coexistence testing. Each baseband generator supports 120-MHz modulation bandwidth with 512M samples of playback memory for simulating long, complex signals. This approach enables earlier identification of problems, which allows you to reduce uncertainties, minimize rework, and shorten time to market.

Seamless signal routing and automated power calibration minimize test time and eliminate the time-consuming system setup previously required for fading and multiformat coexistence-signal summing. Predefined test configurations further reduce test time and allow you to quickly define complex instrument settings. A GUI (graphical user interface) with drop-down menus speeds learning and provides quick selection of test settings such as MIMO-channel models and path configurations.

The tester features a scalable, high-performance platform based on a field-upgradable architecture. Adding support for the test needs of future technologies, such as 4G (fourth-generation) and higher-order MIMO implementations, requires only a cost-effective upgrade that you can perform in an hour. The architecture extends the instrument's service life, maximizes your equipment investments, and reduces the cost of test by allowing you to use existing Agilent signal generators and analyzers and other RF-test equipment. Pricing depends on the system configuration and begins at $31,000.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/PXB.

DILBERT By Scott Adams

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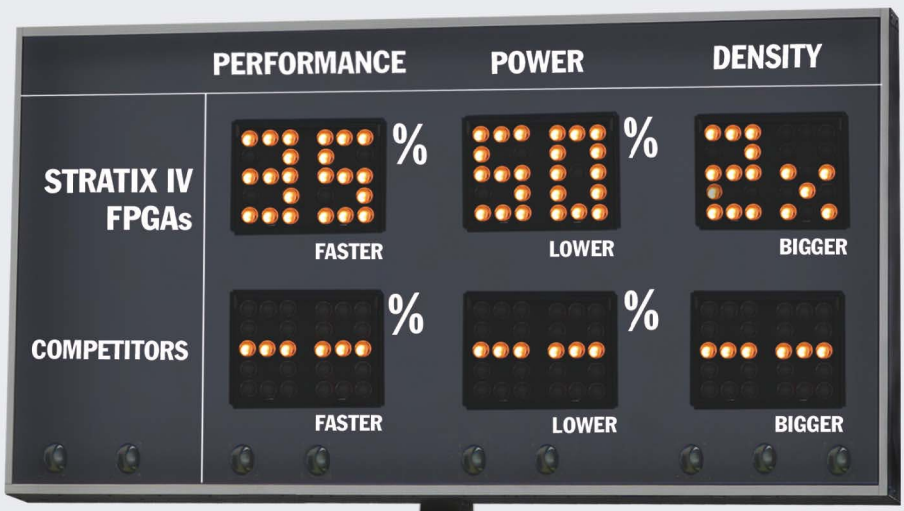

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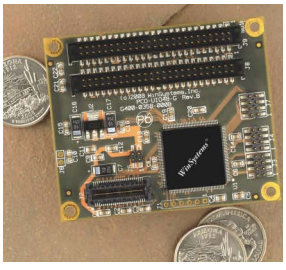
Tiny module delivers Pico-ITXe expansion

As standard off-the-shelf board architectures shrink, designers need simple and low-cost techniques to tack on custom I/O. Toward that end, WinSystems recently introduced the first Pico-I/O module for expanding Pico-ITXe single-board computers. The 48-point PCO-UIO48-G digital-I/O interface has an interruptible event sensor. The card monitors 24 of the rising and falling digital-edge transitions, latches them, and then signals the host processor that a change of input status has occurred. This approach is the most efficient way of sensing and signaling a CPU of real-time events without the burden of continuous polling of the digital-I/O points.



The first Pico-I/O expansion module from WinSystems provides 24 event-sense lines and eliminates the time-consuming burden of polling digital I/O.

WinSystems based the PCO-UIO48-G's I/O controller on a Lattice (www.latticesemi.com) FPGA programmed to support various I/O and interrupt configurations. Each I/O line is programmable for input, output, or output with read-back operation. Each line's transition is latched so that the module recognizes even short pulses. A Pico-I/O module measures 60×72 mm, which is approximately half the area of a PC/104 module. The Pico-I/O employs the SUMIT (stackable-unified-module-interconnect-technology) connector, which the SFF-SIG (Small Form Factor Special Interest Group, www.sff-sig.org) developed. The PCO-UIO48-G has a list price of $59 and is available from stock to two weeks.

—by Warren Webb

▷**WinSystems**, www.winsystems.com.

EDN BLOG

BRIAN'S BRAIN

Intel's SLC SSDs: the rest of the story

Oh, how I detest multiphase product introductions. ... Ahem. Back in mid-August, Intel unveiled its MLC (multi-level-cell) and SLC (single-level-cell) flash-memory-based, 1.8- and 2.5-in.-solid-state-drive plans, and, several weeks later, the company followed up with pricing and a "we're-shipping-now-so-order-away" green-light-status announcement on the MLC variants.

Now, it's the 2.5-in. SLC drives' turn for a wrap-up update. The 32-Gbyte drive, now in production, sells for $695 (1000).

The 64-Gbyte version will be sampling this quarter, "with production estimated for the first quarter of 2009."

I tried to get firmer sampling and production dates from my Intel contacts, warning them that, in the absence of more definitive data, your assumed actual sampling date would be New Year's Eve, 11:59:59 pm ... but no such luck.

Don't be too hard on the company, though; after all, it beat the original "within-90-days" SLC-SSD (solid-state-drive) production-shipping estimate by more than a month!

And the product performance estimates originally touted in mid-August haven't slipped, either, as far as I can tell:

- 75-µsec read latency,
- 2.4W active-power consumption,
- 250-Mbyte/sec peak sequential-read speeds, and
- 170-Mbyte/sec peak sequential-write speeds.

Take a look at my recent hands-on feature article "Solid-state drives challenge hard disks" (*EDN*, Nov 13, 2008, pg 25, www.edn.com/article/CA6611643).

Among other things, the article tested Intel's MLC SSDs in both single- and dual-drive RAID 0 configurations. Those results and others appear on *Brian's Brain* as an online addendum to the print piece.

—by Brian Dipert

▶www.edn.com/briansbrain.

▶For the full post, go to www.edn.com/081205ba.

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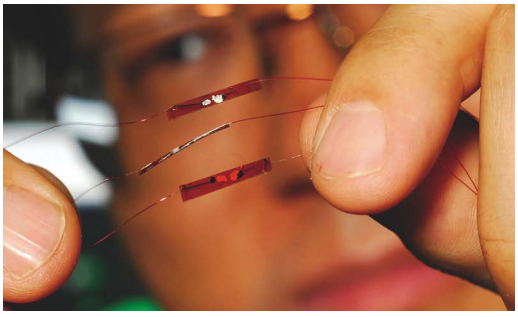
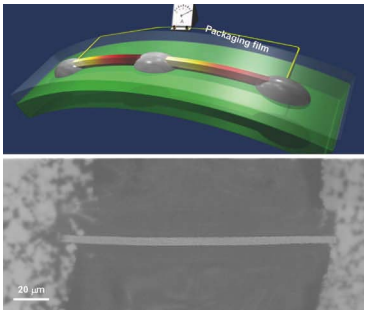
ANALOG DEVICES

RESEARCH UPDATE

BY FRAN GRANVILLE



Team leader Professor Zhong Lin Wang displays flexible charge pumps that can produce ac current through the stretching and relaxing of zinc-oxide wires (courtesy Gary Meek, Georgia Institute of Technology).



The flexible charge pump produces ac current by stretching zinc-oxide wires (top). A micrograph shows an actual prototype (bottom).

Flexible charge pump offers another means of producing electricity

Researchers at the Georgia Institute of Technology have developed a new type of small-scale electric-power generator that produces ac current through the cyclical stretching and releasing of zinc-oxide wires encapsulated in a flexible plastic substrate with two bonded ends.

The generator produces an oscillating output voltage as high as 45 mV, converting nearly 7% of the mechanical energy applied directly to the zinc-oxide wires into electricity. Potential applications include medical sensing, environmental monitoring, defense technology, and personal electronics.

The team previously developed nanowire nanogenerators and microfiber nanogenerators that depended on either intermittent contact between vertically grown zinc-oxide nanowires and an electrode or the mechanical scrubbing of nanowire-covered fibers. These devices were difficult to construct, and the mechanical contact required caused wear that limited how long they could operate. And, because zinc oxide is soluble in water, they required protection from moisture. The new charge pump resolves these issues.

When the researchers mechanically stretch and then release the modules, the piezoelectric properties of the zinc-oxide material allow it to generate a piezoelectric potential that alternately builds up and then is released. The researchers grow the wires using a physical vapor-deposition method at approximately 600°C. Using an optical microscope, they bond the wires onto a polyimide film and apply silver paste at both ends to serve as electrodes. They then encase the wires and electrodes in polyimide to protect them from environmental degradation.

▷**Georgia Institute of Technology**, www.gatech.edu.

ENGINEERS DEVELOP ATOMIC-SCALE COMPOSITIONAL IMAGES OF FUEL-CELL NANOPARTICLES

Engineers at the Massachusetts Institute of Technology, the University of Texas–Austin (www.utexas.edu), and the Oak Ridge National Laboratory (www.ornl.gov) have taken the first images of individual atoms on and near the surface of nanoparticles. The researchers treated platinum and cobalt nanoparticles with acid or treated them with acid and then subjected them to high temperatures. In the nanoparticles subjected to heat treatments, the platinum and cobalt atoms formed a sandwich-like structure. Platinum atoms covered most of the surface, and the next layer down was composed primarily of cobalt. Successive layers contained mixtures of the two. The team believes that these nanoparticles are as much as four times more active than platinum alone because the cobalt below constrains the platinum above.

Read more at http://web.mit.edu/newsoffice/2008/fuel-cell-1002.html.

▶MIT, www.mit.edu.

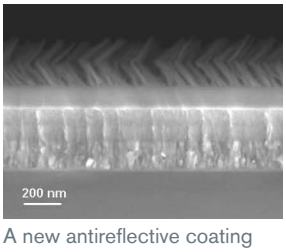
Coating provides near-perfect absorption of sunlight from all angles

Researchers at Rensselaer Polytechnic Institute have developed an antireflective coating that boosts the amount of sunlight that solar panels can capture and allows the panels to absorb the entire solar spectrum from nearly any angle. The development moves the industry closer to the realization of high-efficiency, cost-effective solar power.

After treating a silicon surface with the new reflective coating, the researchers found that the material absorbed 96.21% of the sunlight—versus 67.4% with untreated silicon—meaning that only 3.79% in the new process goes unharvested.

The coating also absorbs sunlight evenly and equally from all angles—unlike eyeglass lenses or conventional solar panels, for example, which depend on the source of the light and the position of the sun. Thus, a stationary solar panel treated with the coating would absorb 96.21% of sunlight, no matter the position of the sun in the sky.

▷**Rensselaer Polytechnic Institute**, www.rpi.edu.



A new antireflective coating boosts the amount of sunlight that solar panels capture and allows those panels to absorb the entire spectrum of sunlight from any angle (courtesy Shawn Lin, Rensselaer Polytechnic Institute).

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BY HOWARD JOHNSON, PhD

Visualizing differential crosstalk

Figure 1 depicts two 100Ω differential pairs of PCB (printed-circuit-board) traces. A solid-plane layer appears at the bottom of the **figure**. An upper solid plane exists somewhere above the **figure**. This plot shows only a subset of the full stripline cross section.

A pattern of thin, colored lines represents the magnetic field resulting from current in the left-most pair. Technically, the lines prescribe contours of constant 2-D magnetic scaler potential. The magnetic field is most intense where the lines fall closest together and least intense on the right side of the diagram where the lines spread far apart. The field intensity proximate to the conductors appears very intense. Pixelation effects in the **figure** may create what look like moiré interference patterns in the dense region. The moiré patterns are not real. The field patterns proximate to the conductors form a set of concentric curves near the surface of each tiny conductor.

You can estimate the crosstalk picked up by the victim pair, wires A and B, based on the field patterns in this diagram. Your estimate will not be perfect because the mere presence of wires A and B will distort somewhat the high-frequency magnetic-field pattern, but the general principle remains quite useful. Simply count the number of magnetic-field lines that pass between wires A and B to estimate the crosstalk picked up between them.

There are 96 magnetic-field lines between the two conductors on the left side. You can't see those lines, but I know how many there are because I wrote the code that generated this **figure**. There are three lines passing through the flux window between the centerlines of victim traces A and B. Near-end crosstalk is simply the ratio of 3 to 96—about 3%. That's all there is to estimating crosstalk.

Experts in electric- and magnetic-field calculations may recognize that my procedure takes into account only magnetic-field effects, ignoring capacitive coupling. The procedure still works because, in a stripline configuration, inductive- and capacitive-coupling effects are nearly always exactly equal. Compute one, and you have the other.

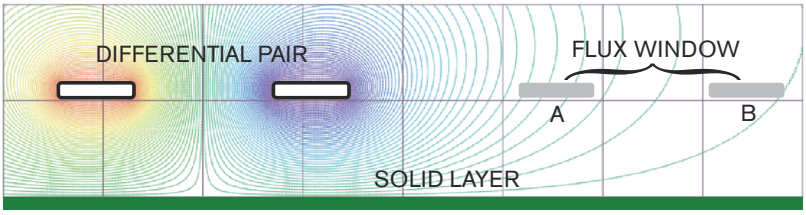

Figure 1 The number of lines of magnetic flux passing between traces A and B indicates crosstalk.

Now, change something. Grab traces A and B and move them both to the left by about one-half a trace width. In response to that action, two new magnetic lines of force now fall within the victim's flux window. Crosstalk increases to 5%, almost double the previous result. The spacing between the aggressor pair and the victim pair greatly affects crosstalk.

Put the traces back to their original positions and try again. This time, leave trace A in its original position while you bring B to the left by one-half a trace width. After you slide B into its new position, three flux lines still penetrate. Crosstalk hardly changes. In a more accurate plot, you would surely observe some small effect, but I think you get the picture. The spacing between the wires of a differential-stripline pair only mildly affects crosstalk.

In this example, the spacing between wires A and B has little effect because the crosstalk effect is not well-balanced. The aggressive field affects wire A much more strongly than it affects wire B. Differential systems can reject only the noise that equally affects both wires. In a nonsymmetric situation, differential-noise cancellation does not occur.

I hope **Figure 1** helps you visualize why differential PCB traces do not significantly reduce crosstalk from other traces. To reduce intertrace crosstalk, you must enforce spacing rules between the aggressor and the victim, much as you would with single-ended signals. EDN

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Mentor's new DRC tool targets 32-nm node

Mentor Graphics is enhancing its market-leading Calibre physical-verification environment for subwavelength-semiconductor processes with Calibre EQDRC (equation-based design-rule checking). The equations can be multivariable statements, which Calibre calculates dynamically using other measurement criteria, as part of the DRC. Traditional DRC programs have short-range, fixed-condition, single-measurement-value rules (**Table 1**, available in the Web version of this column at www.edn.com/081205pc). Designers typically use these rules for 0.35-µm or larger-geometry processes.

Combinations of rule- and model-based rules are typical for 0.25-µm to 65-nm process technologies. Conditional, critical-area-analysis, and complex-2-D rules, as well as staggered "if-then-else" loops, validate geometry in these technologies. Using all these types of rules has led to an explosion in the size of the runtime code to support complex, multilayer, and multiproperty design rules. In larger processes, this type of rule was the exception, but, in 45-nm and smaller processes, it is the norm.

Mentor created the Calibre EQDRC environment to optimally support 32-nm processes and validated the rule sets with a major commercial-32-nm-CMOS-process foundry. The company is not unique, however. Synopsys also implemented an addition, targeting the 45-nm node, to its runtime syntax for the Hercules DRC/LVS (layout-versus-schematic) tool. No one knows when or whether customers will adopt any geometry smaller than 45 nm, however.

Thanks to its support for multivariable-mathematical expressions, the new syntax supports complex-rule implementation with significantly less code. The syntax also allows for systematic support of implicit and suggested design rules. As a result, designers can test the guidelines for multivoltage designs, latch-up resistance in multipower-state designs, and core-I/O-stacking rules.

Figure 1 shows a typical application of a simple mathematical solution and runtime coding for a spacing rule that involves CMP (chemical-mechanical-polishing) dishing and metal spacing. This approach replaces more than 50 lines of SVRF (standard-verification-rule-format) coding and has a faster runtime in a smaller memory footprint than standard coding. Another example from Mentor replaces more than 3000 lines of customer-derived runtime code with fewer than 30 lines of enhanced coding to support alignment of vias and via-count rules. Most of the applications address application DFM (design-for-manufacturing) and lithography prescreening rules.

Because the rules do not directly relate to the design objects, multiple conditions may be at work for the design checks, meaning that error reporting also changes. The tool not only flags the offending object—that is, the edge, vertex, or polygon—as an error but also highlights repair options. For instance, the tool may base a position rule on an edge location, an overlap, or a corner rule and present all three repair options so that the user can choose the most appropriate one for the design application. This feature should significantly reduce the debugging time and learning curve for new processes for the physical-design staff. EDN

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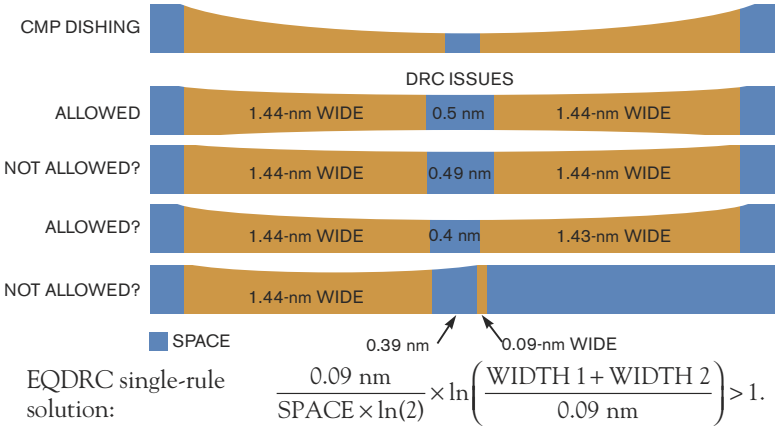

Figure 1 With EQDRC, you can replace more than 50 lines of standard coding with one rule.

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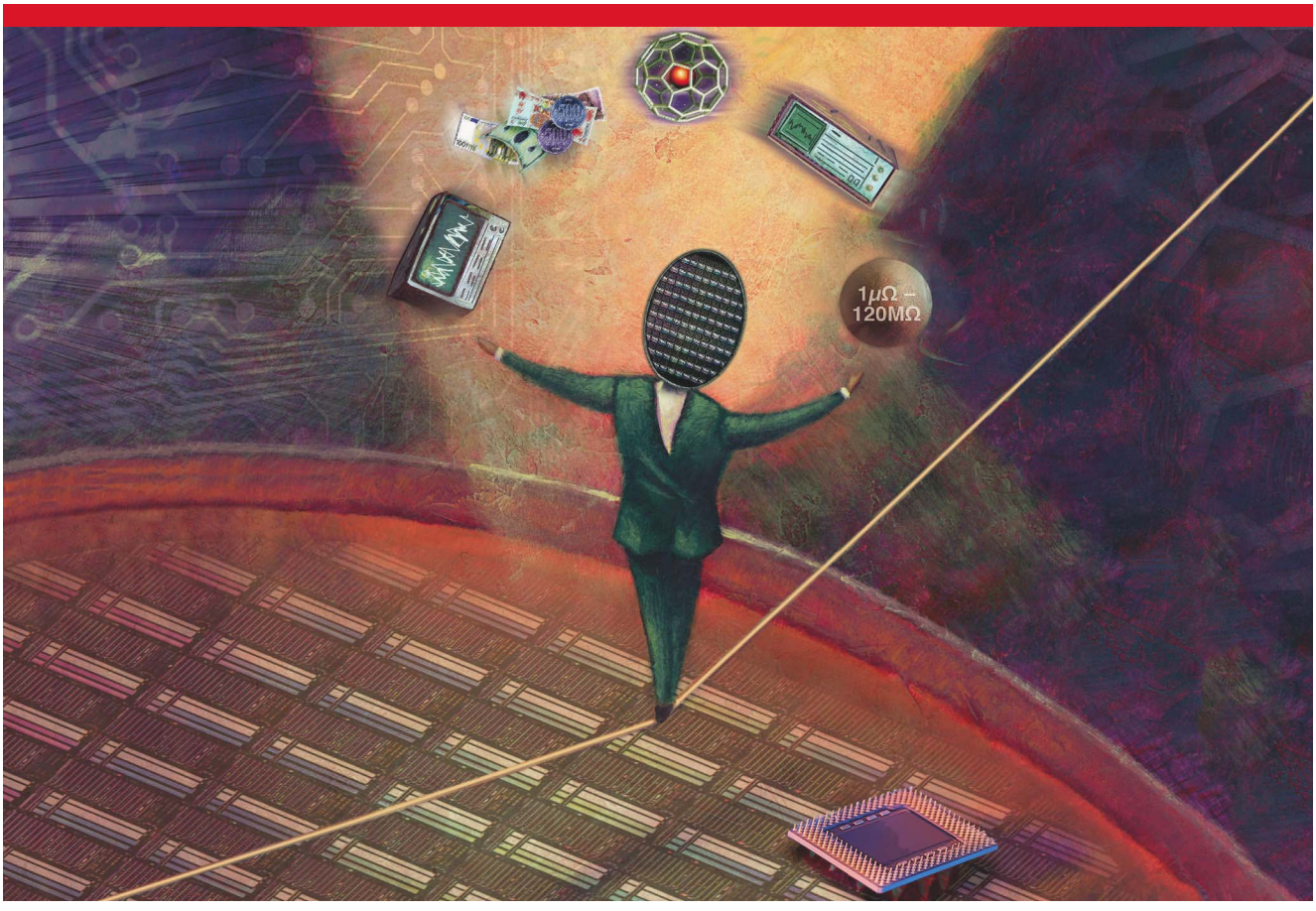

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COLLECTING VERIFICATION-COVERAGE METRICS AND FUSING THEM INTO A CLEAR PICTURE OF WHERE YOU STAND IS NO EASY MATTER.

BY RON WILSON • EXECUTIVE EDITOR

VERIFICATION METRICS: WHEN IS ENOUGH ENOUGH?

Today, most design managers depend on some sort of verification-coverage metrics to answer three primary questions, according to Mentor Graphics' chief verification scientist, Harry Foster: Where have I been, where am I going, and when will I get there?

But there are many coverage metrics, coming from various tools and meaning different things. It is vital for design managers to understand what each sort of metric really means. Equally important, the manager must be able to blend a variety of metrics into one picture that will answer Foster's three questions. Most important, the manager must answer correctly another version of the third question: When is it time to stop? The decision not only requires a fusion of diverse metrics, but also depends upon a detailed verification plan that has existed since the early days of the architectural design and has since grown and blossomed right along with the design.

The idea of code coverage, which designers borrowed from identical tools in the software-verification world, is simple: As you run RTL (register-transfer-level) simulation, you simply maintain a 1-bit-wide table with an entry for each line of code in the RTL source. At the beginning of a simulation run, you set the bits in the table to zero. The first time you execute each line, you set the corresponding bit in the table to one. When you end the simulation, you have a map of which lines of code you executed and which you did not. If you did not execute a line, it is safe to say you did not verify it.

Experts generalize the notion of code coverage to lots of other implicit measures of coverage based on the RTL view of the design. You can devise tools that report on coverage of RTL expressions, branches, or toggling of registers. And most such reports are readily available from commercial simulation tools without your having to devise special monitors.

The early appearance of code-coverage metrics and their ease of use have made them popular. Foster says that Mentor's survey data indicate that about half of design teams have code-coverage metrics somewhere in their verification flow. But there are serious issues with code coverage, as well. The primary one, says Synopsys fellow Janick Bergeron, is that "structural coverage metrics are necessary, but they are not sufficient to determine verification coverage." Bergeron points out that the

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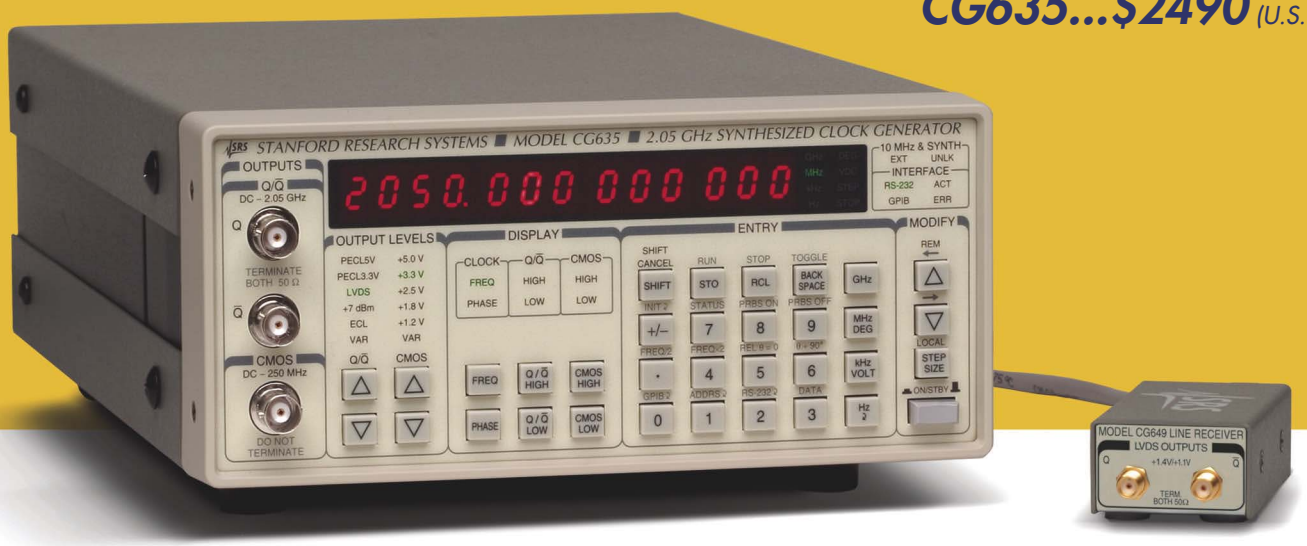

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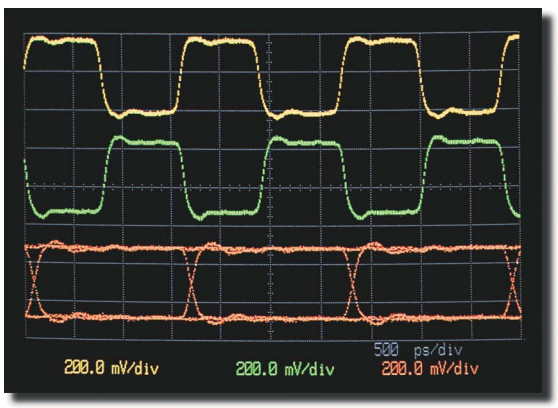

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most glaring issue with code coverage is a logical one. The fact that you have executed a line of RTL doesn't imply that it did what you intended.

More precisely, the problems are of observability and completeness. When you executed this line of code, did its results travel to a node that you were actually observing during this simulation run? If not, then you have no idea whether the code did what you intended. "We have seen designs that have 100% line coverage, but, in fact, the actions of only 70% of the lines were observed during simulation," Foster says.

Completeness is a separate issue. You executed the line of code. But did you execute it in all of the cases in which it can be active? How about the one case in which it doesn't work?

FUNCTIONAL METRICS

These shortcomings have led many teams to use functional verification. Functional coverage asks how many of the functions of the design you have shown to do what you intended. In its intuitive forms, it is the earliest means managers have used to measure verification, and it is the mainstay of many teams.

Hans Sahm, technical manager in hardware research and development at the optical division of Alcatel-Lucent, describes a modern version of this seminal approach. "We start with a requirements document, and we use internally developed scripting to generate a verification-plan spreadsheet from the requirements," Sahm says. "That spreadsheet lists functional requirements, described in English, and the test cases the verification team has chosen to verify each requirement." This spreadsheet gives the verification team a single document in which they can check off test cases as they run in simulation and thereby have a function-by-function chart of verification progress.

This concept forms the backbone of all forms of functional-coverage metrics, but it suffers from some serious challenges. As Sahm points out, "There is no automatic link between a functional requirement and the test cases necessary to verify it." Understanding a requirement and translating it into tests that adequately cover that requirement depends on the skill and experience of the verification engineer.

AT A GLANCE

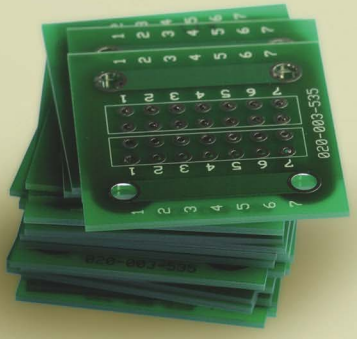
- Design managers depend on verification-coverage metrics to answer the questions of where they have been, where they are going, and when they will get there.
- Functional coverage is the earliest means of measuring verification and is the mainstay of many design teams.
- Different engineers can read the same document and come away with different ideas of how a function should behave.
- Code-, functional-, and assertion-coverage metrics all leave some unanswered questions.
- You stop verification when you are virtually certain of the critical blocks.

"There is no automation for thinking," says Mentor's Foster.

"There is always a problem with interpreting the requirements documents," says Jeff Fox, principal verification architect at Altera. "Different engineers can read the same document and come away with quite different ideas of how the function should behave. That is why we try to keep our requirements documents as close as possible to executable code. They must be precise."

Synopsys' Bergeron agrees. "When you create directed tests to verify a function, it is an open-loop process," he observes. "You can never be sure from the result that there isn't a bug in the test."

The most common technique for combating this reliance on human frailty has been the use of assertions and constrained random testing, as Verisity, which Cadence now owns, originally championed. According to Mentor's survey data, only about 40% of verification teams are using constrained random tests. Correspondingly, about 40% are using functional-coverage metrics. Since the early days, a number of specialized languages have appeared in which to write assertions, but the industry now appears to be converging on System Verilog for this purpose. So, we are seeing a new pattern: assertions in System Verilog, constrained random tests to test the assertions, and verification metrics expressed as coverage of the assertions.



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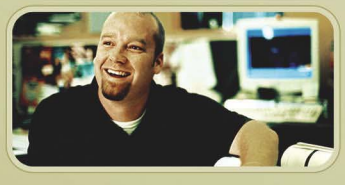

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This process is evolutionary for many design teams. Giri Raju, general manager of the semiconductor- and solutions-business unit at Wipro Technologies, describes the path his design teams are taking. "Previously, we had used only code-coverage metrics, tracked in a manual cross-reference table, to manage verification," he says. "Our goal was simply 100% code coverage. In stages, we have moved to functional-verification tools, and we have continued to track the progress of verification with the manual tables. Now, we are moving to System Verilog and the Open Verification Methodology.

"There is still much engineering skill required. Verification engineers identify coverage points for verification, and review them with the design engineers as a check. We believe we can automate 80 to 90% of this process, but there will al-

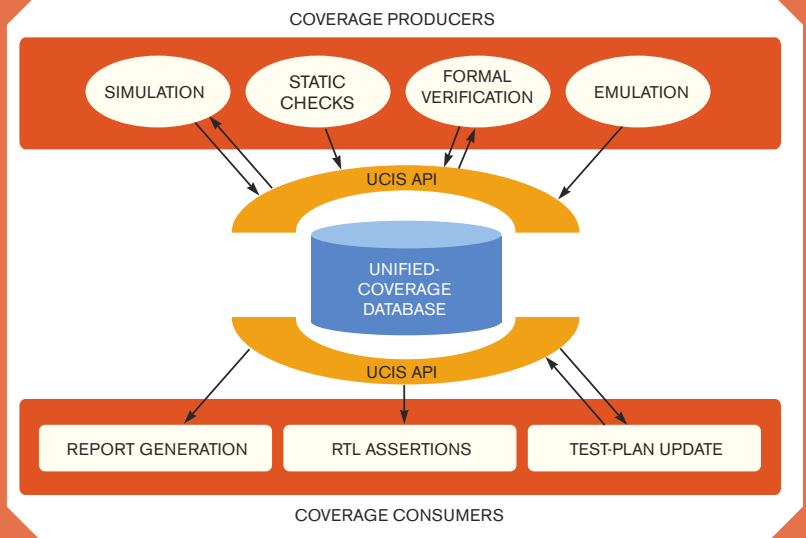

Figure A Coverage metrics come from many tools, and several kinds of clients consume them.

UCIS ENSURES INTEROPERABILITY

By Harry Foster, Mentor Graphics

Today's contemporary verification flows often employ a diverse set of verification tools, ranging from various forms of simulation to formal verification and even emulation. Each of the processes might generate multiple coverage metrics, which you use to measure the effectiveness of a process and highlight shortcomings that might require attention.

The issue with today's flow is that any tool within a process might generate coverage metrics that are disjointed, overlapping, or a subset of metrics that a different tool might generate. Further, each tool generates its coverage data in a vendor-specific format. Managing this diverse set of coverage data for analysis can be a nightmare for even the most sophisticated project team.

Accellera created the UCIS (Unified Coverage Interoperability Standard) to ensure interoperability when gathering, merging, and interpreting coverage results across a multitool heterogeneous verification flow (Figure A). By using the future Accellera UCIS API (application-programming-interface) standard, multiple verification tools will be able to access a UCDB (unified coverage database), which you can view conceptually as single repository of all coverage data.

AUTHOR'S BIOGRAPHY

Harry Foster is chief verification scientist at Mentor Graphics.

ways be certain scenarios where things have to be worked out manually. Assertions really help us, though. Our design engineers are now used to inserting assertions in their code."

One great boon to the process of generating assertion-coverage metrics has been the use of FPGAs (field-programmable gate arrays) for logic verification in a System Verilog environment. Newer tools allow verification engineers to generate constrained random stimulus patterns, and the tools then track hits on coverage points. FPGAs can enormously accelerate this process, Altera's Fox says, by allowing the team to synthesize the design and the assertions and run tests at or near actual real time. This approach allows the constrained random test creator to cast a much wider net, exploring for not just known but also unknown corner cases.

It also allows for a physical sort of transaction-level coverage. Using an FPGA vehicle, verification engineers can check the operation of an interface, for instance, by simply connecting the FPGA to a known-good external device and watching the transactions. One line of reasoning goes that, if the interface "plays well" with other chips, it is 100% covered.

FORMAL TOOLS

With code-, functional-, and assertion-coverage metrics, the verification manager has many numbers that suggest the degree of completion of verification. Yet, all of them leave some questions unanswered. Increasingly, some teams are using formal-verification tools as adjuncts to simulation-based techniques. These tools bring their own unique metrics to the table.

"On the most critical modules, we are using formal property-checking tools now," says Alcatel-Lucent's Sahm. "This [approach] introduces the notion of property coverage. Actually, the tool we use has its own internal completeness-checking capabilities that measure such things as coverage of the properties, and whether the state of each output is determined in a given scenario."

In a way, formal tools give the ultimate insurance. At the end of a run, you have before you all of the counter-examples that violate each property you specified. By definition, the property is 100% covered. But there's the question of how completely the set of properties covers the design intent. And, once again, you are back to the skill of the designers, now perhaps reduced because of the notoriously difficult learning curve for the formal-verification tools.

FUSING THE DATA

As you can see, there is no solid answer to verification coverage. Individual tools can tell you how completely they traversed the structure of the RTL code or how fully they checked the assertions

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the design and verification teams wrote or proved the properties the formal-verification expert defined. But a human process of interpretation and creation separates each of these metrics from the design intent. So, many design managers form their picture of verification progress by fusing the coverage metrics from many sources.

"Different teams have different ways of combining the coverage data into a single picture," Foster says. "The CPU guys frequently will use only functional-coverage metrics, but they have the resources to make that [approach] work. Without the resources, some design teams still use only line coverage. But you can combine the different kinds of numbers, as well."

Foster suggests that a team could start with functional-coverage metrics. As the functional coverage approaches 100%, the team could turn on code-line coverage as a check of completeness. This approach, as Altera's Fox points out, allows the team to spot holes in the functional coverage. If a block of code does not get executed, either it is dead code—which the design team should be able to determine by inspection—or there are some functions of the design that are not covered. "At that point, you write some directed tests," Fox says.

Fox emphasizes the importance of having data from different sources. "For instance, we were working on an interface IP [intellectual-property] block recently," he says. "We brought in third-party verification IP from three vendors and put two internal teams on the verification process, as well. Combining the data from all of them found that each approach had overlooked some things."

FINDING THE END

Given experiences such as Fox's, when can a manager say that verification is complete? The cynic would say verification is never complete. The stoic would reply that verification is complete when you overshoot the schedule. The pragmatist has a more interesting answer, however. "You are never 'done,'" Bergeron says. "But you can reach a level of confidence in the functions that are required for commercial success. It's a risk-management question."

Accordingly, Bergeron and Foster say, experienced verification managers watch the coverage metrics from various sources. Commercial tools are available to assist this process by organizing the various metrics by structural block or by function, so verification engineers can look at all the metrics for one area of the design. And efforts exist to ease the fusion process (see **sidebar** "UCIS ensures interoperability"). Discrepancies at this level usually indicate holes in the verification plan that the team should plug with manually created directed tests.

But the manager should also look at the frequency of bug reports. If bug-report frequency is dropping as the coverage metrics near 100%, all is well. If the bugs keep showing up at a constant rate—or worse—then something is wrong. But when do you stop? Most managers agree: You stop when you are virtually certain of the critical blocks. Sahm defines "critical" as blocks containing entirely new functions, blocks that you cannot easily work around in software, and blocks with which the designers lack experience.

"It is a very legitimate strategy to use coverage metrics to attempt to confine the risk in the design to fixable blocks," Foster says. "These blocks may have obvious software workarounds. They may have a bunch of uncommitted gates—we used to call them 'happy gates'—that the designers can use to make patches with just a couple of metal layers. Or the blocks may implement new algorithms that the designers can simply switch off if they don't work.

"Coverage metrics can't tell you on what date you will be done," Foster concludes. "You can watch the coverage curves. If they are flattening out short of 100%, you can change your strategy. If there are big holes in coverage, you can aim your efforts at them. If there are lots of little holes, you may need to change your strategy altogether and maybe try formal methods or a special testbench for the scattered areas. But you watch the metrics to see where you are going, and where you should go next."EDN


You can reach Executive Editor Ron Wilson at 1-408-345-4427 and ronald.wilson@reedbusiness.com.

PROTOTYPING TECHNIQUES:

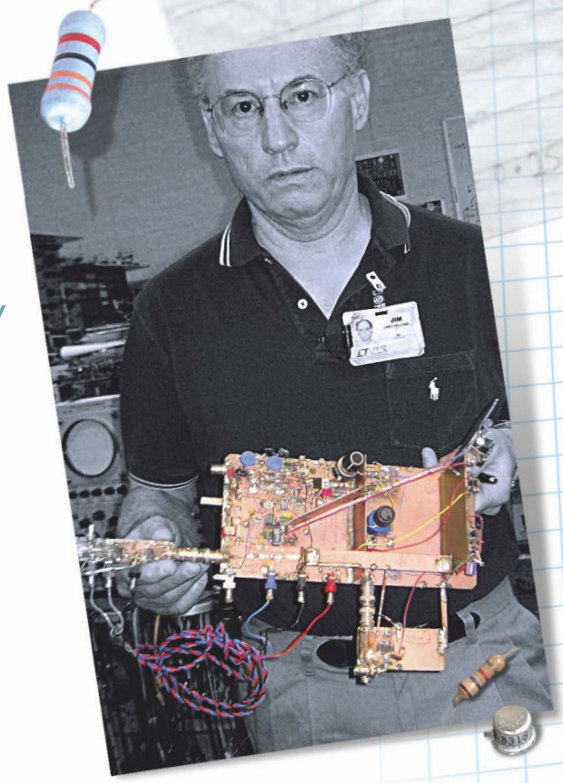
THINGS TO KNOW BEFORE PULLING THE TRIGGER

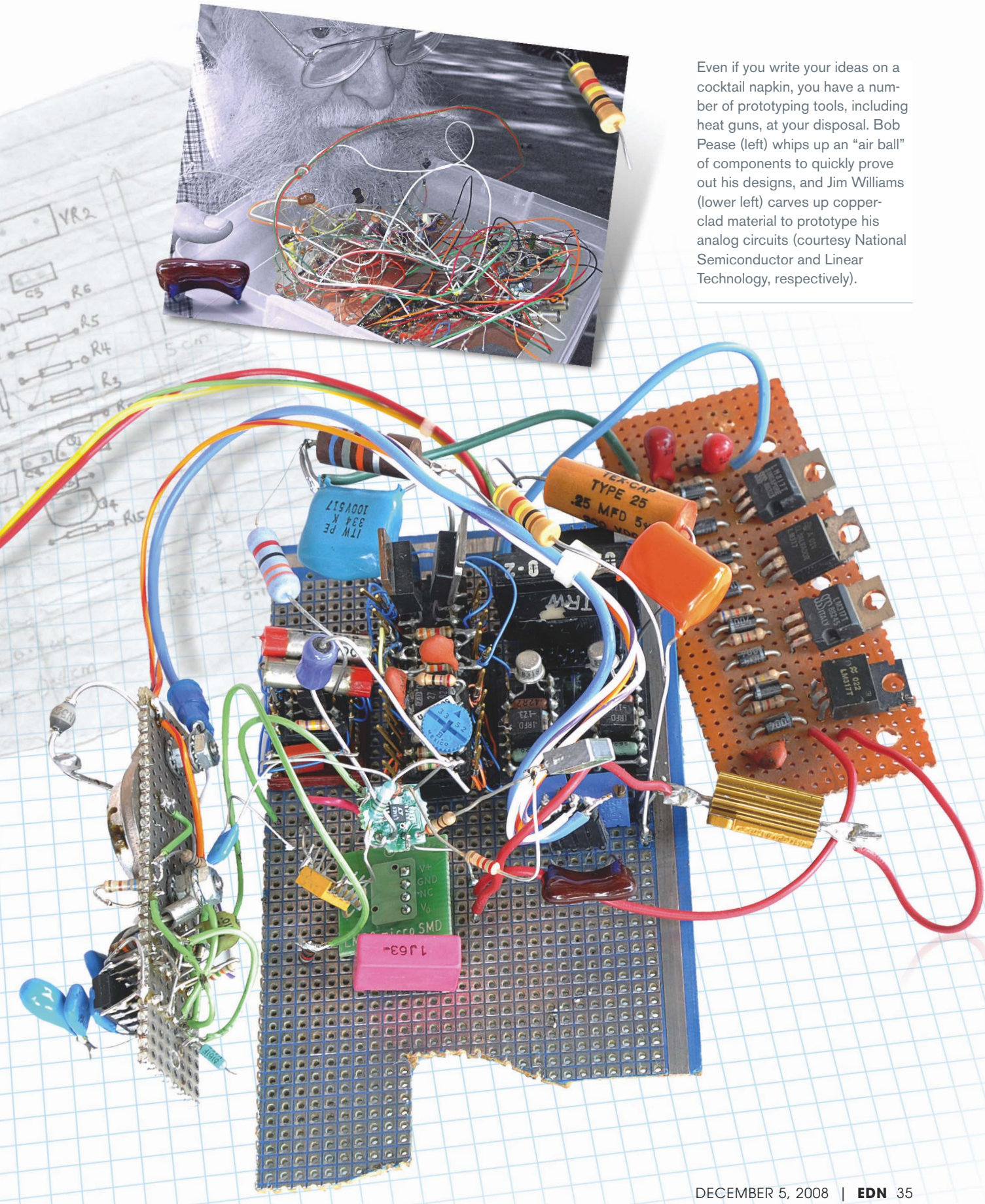
BY PAUL RAKO • TECHNICAL EDITOR

Prototyping has become far more difficult than it was in the old days. For one thing, electronic components have gotten smaller; an IC can now be the size of a peppercorn or a grain of sand. As a result, you must take measures to illuminate, observe, and handle these tiny parts (see **sidebar** "Prototyping: Think small and work smart" with the Web version of this article at www.edn.com/081205cs). Making things even more difficult is the fact that many modern circuits operate at high frequencies, so you can no longer just solder wires between components; you must connect those circuits with controlled impedances using traces. Thermal management brings more challenges.

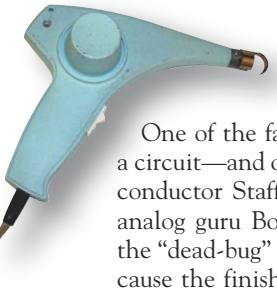
TINY COMPONENTS AND HIGH-FREQUENCY CIRCUITS DEMAND RIGOROUS PROTOTYPING METHODS.

To prototype a PCB (printed-circuit board), you need lamps, tweezers, magnifiers, microscopes, and solder stations. Once you have collected this equipment, you are ready to build your prototype. Remember to take special precautions in the design and layout of analog boards, however (**Reference 1**).





Even if you write your ideas on a cocktail napkin, you have a number of prototyping tools, including heat guns, at your disposal. Bob Pease (left) whips up an "air ball" of components to quickly prove out his designs, and Jim Williams (lower left) carves up copper-clad material to prototype his analog circuits (courtesy National Semiconductor and Linear Technology, respectively).



One of the fastest ways to prototype a circuit—and one that National Semiconductor Staff Scientist and resident analog guru Bob Pease champions—is the "dead-bug" technique, so called because the finished prototype resembles an insect lying on its back with its legs in the air. The technique can use a solid, copper-clad board as a ground plane. You solder the ground pins of the ICs directly to the plane and wire together the other components above the plane. Because the circuit nodes are suspended in the air—hence, the technique's other nickname, "air-ball" prototyping—the stray capacitance is lower than it would be if the nodes were on a board. The disadvantage of this approach is that it makes it difficult to wire together fast circuits with controlled impedances, although you can use twisted-pair and coaxial cable to connect the parts. For tiny IC packages, you can use a converter board from Digi-Key, Mouser, Newark, Allied, Jameco, or another distributor (**Figure 1**). Although Pease's counterpart at Linear Technology, Jim Williams, sometimes uses the dead-bug technique, he prefers to use copper-clad PCB material, cutting off the copper with an X-Acto knife to make the connections.

Another prototyping method is to use perforated Vectorbord, which Vector Electronics introduced decades ago. Start with a perforated board with solder pads (**Figure 2**) or with both solder pads and plated-through holes. Although this material costs hundreds of dollars per sheet, it allows you to make solid solder joints that can withstand a lot of mechanical stress.

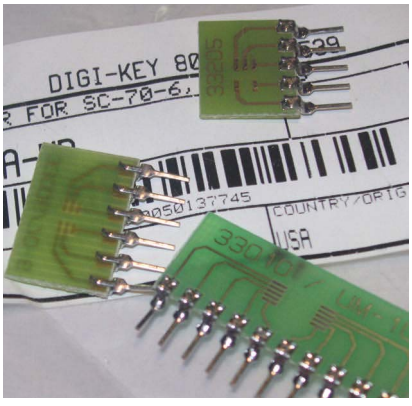


Figure 1 A huge selection of adapter boards spread out tiny packages to 100-mil spacing.

AT A GLANCE

- Modern prototyping requires a full complement of magnifiers, microscopes, lamps, and tweezers.
- "Dead-bug"- and copper-clad-prototype techniques are fast but lack documentation.
- A wire-wrapped prototype is suitable for low-frequency designs.
- Acquiring a board from a fab house gives you a head start.
- Assembly houses can provide quick board turnaround.
- Your job is to deliver a proven documentation package.

A more traditional prototyping technique, wire wrapping, works well for digital designs; you can employ it for analog designs only if there are no fast signals on the board. With the technique, a process that Cooper Hand Tools developed (**Figure 3**), you need to be aware of undershoot problems on the clock. In one case, an engineer spent two weeks trying to figure out why his Z80 processor wouldn't work. He found that the wire-wrapped board had caused 10% undershoot in his design's 4-MHz clock. To fix the problem, he placed a 33Ω resistor in series with the clock circuit to damp out the undershoot. For moderately sized boards, it is worth buying an electric or a manual squeeze-wrap tool rather than spinning the wraps on with a cheap hexagonal barrel tool. You place the unwrapped side of the barrel tool into a drill and use it to unwrap a large number of pins.

Note that, as with all things analog, no one method always works; you may have to combine techniques to get a working design. For example, you might combine sections of copper-clad wiring with areas of dead-bug wiring along with premade demo boards and wire-wrapped areas. You need not use any of these techniques if you can obtain a demo PCB from an IC manufacturer or a reference design from a distributor, such as Avnet.

If the board has more than a dozen traces, you cannot carve it into copper-clad material. However, copper-clad boards with preapplied photoresist are available from many companies. With photoresist, a light-sensitive material for forming a patterned coating on a surface, you can make films for building two-sided PCBs. The only other tools you need are a darkroom and a laser printer. Be sure to flip the image in your computer so that when you place the art over the photoresist, the laser-toner side presses directly against the photoresist; this approach produces crisper lines. Many companies, including Injectorall, offer both precoated boards and photoresist that you apply to boards yourself.

Another method of prototyping requires no photoresist. You use a laser printer to apply the artwork toner to a special plastic film and press the toner side of this film to a copper-clad board. This toner-transfer method requires heat from an iron or a hot plate; the heat from this equipment transfers the toner on the plastic-film artwork to the board. You can rub a ferric-chloride-soaked sponge over the copper to etch off the exposed copper adhering to the board—a faster copper-removal method than agitated tanks can achieve.

The inventor of this rubbing process, Frank Miller, founder of PCB-fabrica-

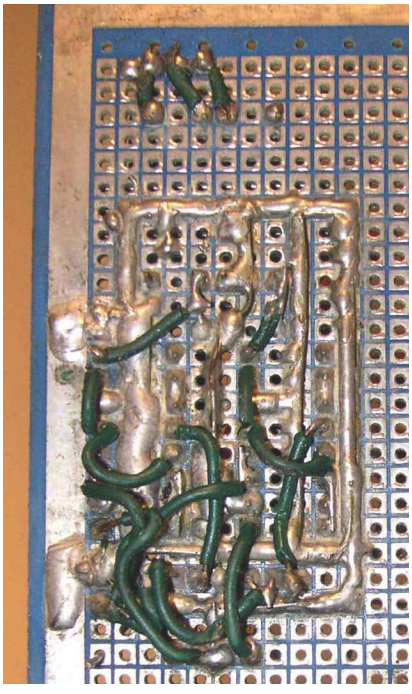


Figure 2 Soldering discrete wires to parts on a perforated board is an acceptable way of prototyping circuits.

tion-supply company Pulsar, also added a step to the photoresist process in which a second transfer seals the material. "The key is a hot-roller laminator and the second application of TRF [toner-reactive foil], which adds strength to the toner and allows for direct rub in the etch process," says Wayne Yamaguchi, owner of Yamaguchi Consulting and a proponent of Miller's method. "The etch time with direct rubbing is now a minute or two."

PROVING OUT THE PROTOYPE

Making boards with CAD (computer-aided-design) files proves the validity of your files early in the design process, so fewer problems emerge when your circuit enters production. The toner-transfer method requires etching and hand drilling. You can also use milling techniques to make your board. LPKF, for example, produces mills such as the one in **Figure 4** that can prove out your Gerber and drill files. Prices for the device start at $11,900, including software that converts conventional Gerber files into milling-machine-tool paths that isolate the traces from each other. Running the mill tool through those parts of your board with 100-mil (0.001-in.) spacing between traces reduces those spaces to 10 mils. For RF designs in which the shape and proximity of the copper are important, you can set the mill software to precisely replicate the trace isolations. In this mode, the mill operates in raster fashion—systematically sampling a grid pattern of pixel spaces to represent an overall image—over any large areas of copper that the mill removes. This process takes longer than it does to simply isolate the nets from each other in one pass.

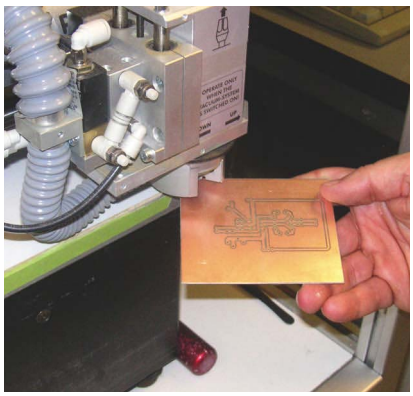


Figure 4 This LPKF mill can route out prototype boards in less than an hour (courtesy National Semiconductor).

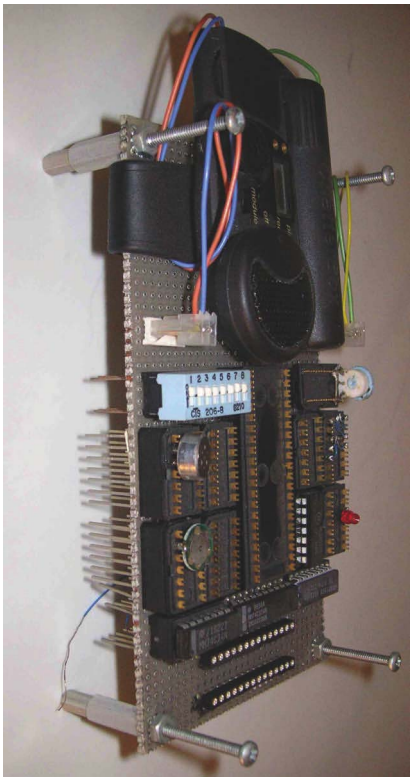


Figure 3 Because of low operating frequencies, wire-wrap techniques work well in this toy-watch-recorder prototype.

The mill can in a matter of hours put a complex prototype into your hands. Using a mill, you make further cuts until a trace achieves the proper impedance. Note, however, that drilling between the layers cannot make a via connection; you must solder a small wire in the via's holes to achieve connectivity. LPKF offers a package that fills the vias with conductive epoxy and supplies small plating tanks for creating multilayer boards. Find out whether your employer requires vent hoods or hazardous-materials handling of these materials. If your company requires a million-dollar facilities investment for a small plating tank, you will need to deal with the conductive epoxy or soldering wires in the vias.

INTO THE BOARDING HOUSE

After you use some or many of these prototype techniques, a board will eventually emerge. Using dead-bug components and X-Acto knives on copper-clad materials provides proof-of-concept

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checks. If you need to make a product, however, you are almost always better off starting a board design in your CAD package rather than soldering components together without documentation. John Massa, consultant at Datadog Systems, points out that, in his 47 years of experience, every project has always come down to the PCB layout and prototyping. "There is rarely a downside to paying for quick-turnaround boards," he says. "You always end up with a better product." Your job is not just to get the circuit working but also to provide a documentation package to manufacturing—whether that manufacturer is your own company or a contract manufacturer in China. Toner-transfer prototypes check out your Gerber files but not your drill files. Milling machines prove out your drill files but do not replicate the silk-screen process. Mills have trouble with micro-SMD (surface-mount-device) packages and other CSPs (chip-scale packages). To make a usable board, you must have a perfectly set up mill that is in good condition.

All these constraints make a good case for sending your board design to a PCB-fabrication house (**Figure 5**). PCB fabrication has in 10 years gone from taking weeks and thousands of dollars to taking 24 hours and hundreds of dollars. Dozens of reputable PCB shops can in a few days turn your CAD files into a board. However, a few companies stand out in their efforts to serve engineers. One that does, Sierra Proto Express, makes two or three boards from your files, delivers them in a few days, and charges less than $200. According to Sierra's owner, Ken Bahl, a need for fast-turnaround prototypes emerged in the early 1990s. By 1996, the managers at PCB-fabrication house Advanced Circuits also realized the benefits of quick-turnaround prototypes. Another pioneer, Sunstone Circuits, had previously been the exclusive board producer for Tektronix. These companies can all provide two-layer boards in a day, as well as multilayer boards in a few days, but each emphasizes a different aspect of the prototype service.

Advanced Circuits touts on-time delivery. "We maintain redundant machinery for the entire process," says Larry McQuinn, vice president of sales and marketing. "If one machine breaks, we can still get you your order on time." Advanced also provides online, real-time DRC (design-rule checking). You can upload your files to a server, and, within hours, you will receive a report detailing shortages or manufacturing problems. This approach prevents your losing a day or more when the fab house finds a problem and has to halt work while you make a change. Advanced also offers the free PCB Artist layout tool, which creates all the files you need for single-layer and multilayer boards.

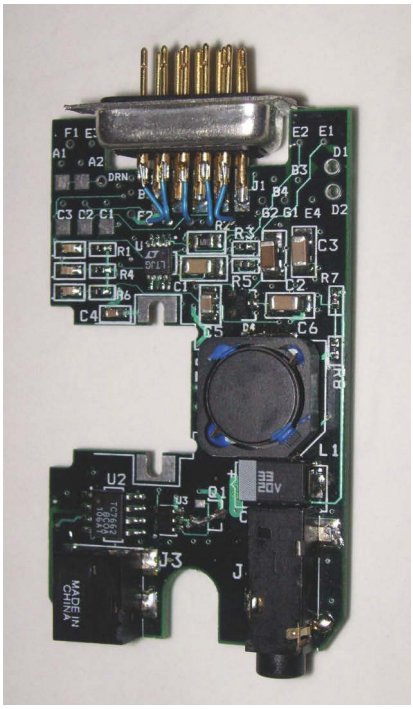

Figure 5 Only a board house can make small boards with fine trace widths and spacings.

Sierra Proto Express has taken another tack: extending the technology in its prototype boards (**Figure 6**). The company can routinely produce boards with lines as narrow as 3 mils. The company also takes on jobs with 2-mil lines and spaces, buried and blind vias, and laser drilling that allows the buried and blind vias to reside on arbitrary and overlapping layers. Although the company provides copper layers as thick as 6 oz, sensible engineers know that they can't expect 2-mil spacing and 6-oz-thick copper on the same board. Sierra can also provide 62-mil-thick, 14-layer boards and thicker boards with as many as 30 layers. Features can include 1-mil-diam-

Figure 6 A PCB-fabrication shop expends huge efforts to electrically and optically inspect your board (courtesy Sierra Proto Express).

eter test pads and state-of-the-art finishes and laminates.

Sunstone is also far from being a bare-bones single-layer-fab shop. The company offers quick-turnaround prototypes and the free PCB123 CAD tool. The company has also developed DFM (design-for-manufacturing) plug-ins for popular layout packages, such as Altium's Designer and Cadsoft's Eagle, that you can set for the appropriate Sunstone design rules. These packages flag any mistakes you make as you are designing the board. Sunstone also works with Screaming Circuits to assemble your board. The company's CAD package can do price checks from Digi-Key, and Sunstone can save shipping and logistics by overseeing the assembly of your boards.

Although these three US companies meet all local, state, and federal standards for pollution control, you can also find responsible PCB fabrication offshore, such as from PCB-Pool, an Irish company that has been making prototype boards since 1994. The company charges by the panel and does not charge for routing, so if you have many small boards requiring routing, PCB-Pool is a good option. The company does charge for the silk-screening and solder-masking options, but the prices are competitive.

ON TO ASSEMBLY

Now that you have a prototype board, you must assemble it or contract with an assembly house to do so (see **sidebar** "PCB assembly: home-brew or send out?" with the Web version of this article at www.edn.com/081205cs). During your career, you should endeavor to send out at least one prototype board to a fab and have a contract manufacturer build it. The experience you gain will help you understand the vicissitudes and exigencies of manufacturing. The fab houses are ready to help, even if you drew your design on a cocktail napkin, and you will be able to lower design costs because you have an understanding of the manufacturing process. "Having a good board shop is part of your being an innovative company," says Amit Bahl, director of marketing for Sierra Proto Express. Even if you have four months to make a prototype, it is well worth it to have a fab house provide a three-day turnaround on your boards. In that way, your marketing and sales organization will have time to review the product and perhaps get one of your prototypes into the hands of a customer. You will then have the opportunity to make improvements and produce a better version of that board in less than a week. By the time the product comes out, you will have a solid design that does even more than your customer expected. As your competitors are trying to catch up, you can be moving to lower cost or improved performance, staying ahead of the pack all the while. EDN

REFERENCE

"Analog Breadboarding," Analog Devices, www.analog.com/static/imported-files/rarely_asked_questions/moreInfo_raq_analogBreadboarding.html.

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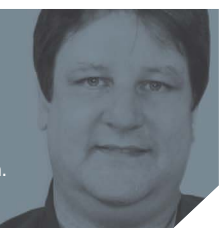

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M25/M45PE	256 B, 4 KB, 64 KB	50 MHz, 75 MHz	1 Mb - 16 Mb

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P30	1.7V - 2.0V, 1.7V - 3.6V	X16 52 MHz Burst	64 Mb - 512 Mb
P33	2.3V - 3.6V	X16 52 MHz Burst	64 Mb - 512 Mb
M29W†	2.7V - 3.6V	X8, X16 Page	4 Mb - 128 Mb
M58BW†	2.7V - 3.6V, 2.5V - 3.3V (55ns)	X32 Burst	16 Mb - 32 Mb

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CompactFlash* card	3V/5V	2 KB	64 MB - 4 GB
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BY PHILLIP HAVENS • LITTELFUSE LP

Designing protective circuitry for DSL loops: Beware of pitfalls

DSL EQUIPMENT REQUIRES PROTECTION FROM A VARIETY OF OVER-VOLTAGE CONDITIONS, BUT THE NEED TO AVOID UNDULY DEGRADING CIRCUIT OPERATION COMPLICATES CIRCUIT DESIGN.

The appropriate protective-circuit design for DSL (digital-subscriber-line) loops depends on the type of loop: Loops vary in voltage conditions and in susceptibility to attenuation and degradation in signal integrity. Therefore, protective circuitry that works well in one application may be completely inappropriate in another. A "normal" signal ranges from 2.5V in an HDSL (high-bit-rate DSL) to 260V in an DSL system (see **sidebar** "Normal signals"). The circuit design and choice of circuit-protection devices must take these differences into account. You should also consider the design with respect to effects of varying capacitance.

BASIC PROTECTIVE CIRCUITS

Designers have a number of devices to choose from—GDTs (gas-discharge tubes), thyristors, MOVs (metal-oxide varistors), and TVS (transient-voltage-suppression) diodes for overvoltage, and fuses and PTC (positive-temperature-coefficient) devices for overcurrent. The challenge is to use them effectively without unduly degrading normal circuit operation.

HDSL circuits require longitudinal protection at both the HTU-C (HDSL-transceiver-unit-central-office) and HTU-R (HDSL-transceiver-unit-remote) interfaces because of the ground connection HDSL uses with loop powering. One approach is to use a pair of TSPDs (transient-surge-protection devices) from tip to ground and ring to ground to provide overvoltage protection, preceding them with a pair of fuses—one on the tip and one on the ring—to provide overcurrent protection (**Figure 1**). For the transceiver side of the coupling transformer, another TSPD can provide overvoltage protection.

The ATU-C (ADSL [asymmetric-DSL]-transceiver-unit-central-office) interface and the ATU-R (ADSL-transceiver-unit-remote) interface typically use longitudinal protection;

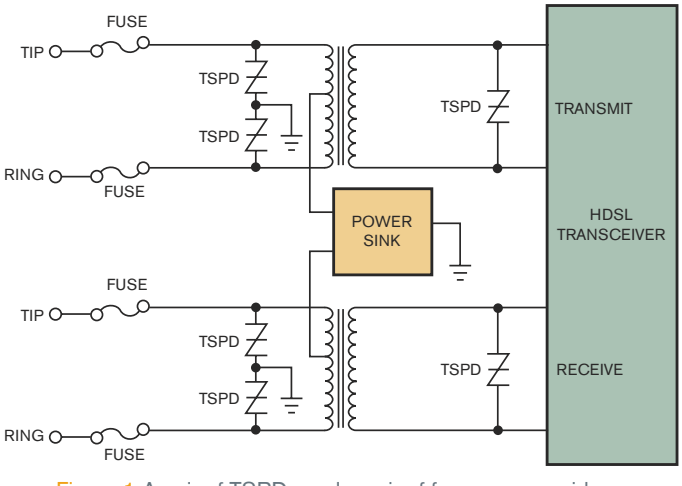

Figure 1 A pair of TSPDs and a pair of fuses can provide overvoltage and overcurrent protection for an HTU-C interface and an HTU-R interface.

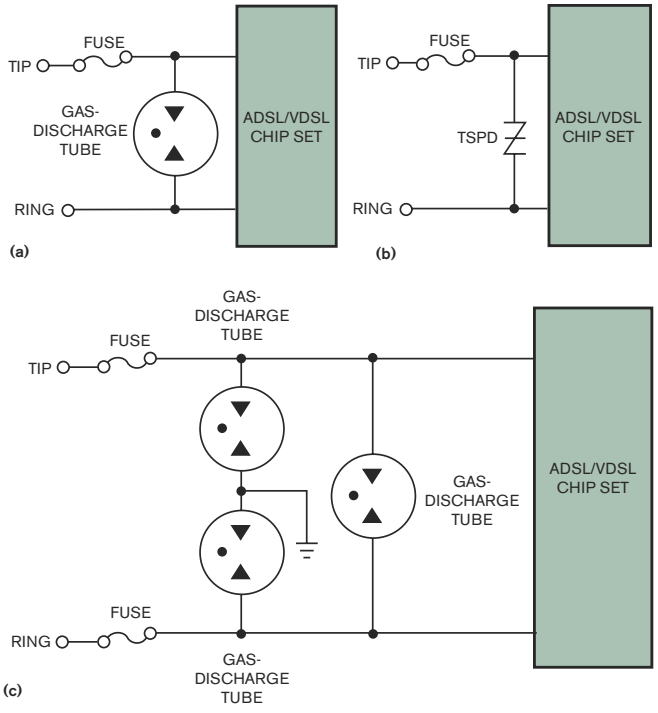

Figure 2 One way to provide metallic protection for an ATU-C interface and an ATU-R interface is to use a simple GDT and a fuse (a). An alternative is to replace the GDT with a TSPD (b). Yet a third method is to connect GDTs in a delta configuration to provide tip-to-ground, ring-to-ground (longitudinal), and tip-to-ring (metallic) protection.

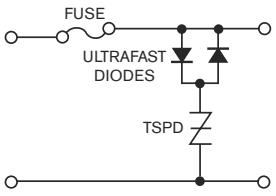

Figure 3 When microcapacitance TSPDs do not sufficiently reduce capacitive effects, a pair of ultrafast-switching diodes in an inverse-parallel arrangement can help in some circuits.

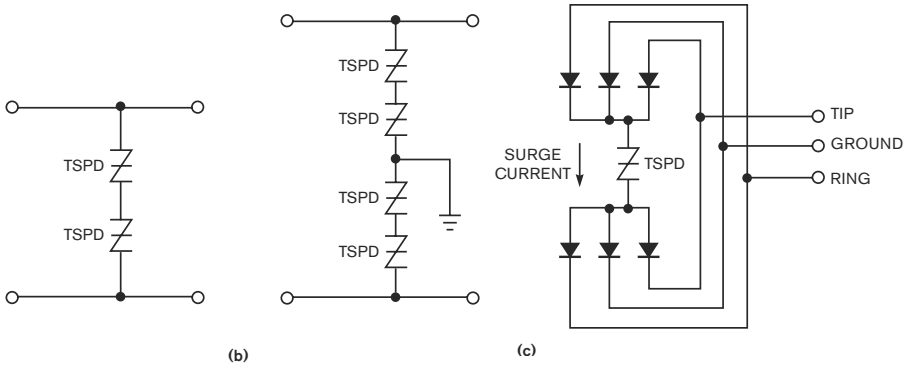

Figure 4 A circuit with two TSPDs (a) works well for metallic transients on CPE. A configuration with four TSPDs works well to protect against the longitudinal surges on ADSL2+ (b). Another useful circuit is a balanced-bridge topology (c).

an ADSL modem at the customer premises does not, due to the absence of earth-ground connections. You may consider a GDT if the design uses a 0.5A fuse (**Figure 2**). A TSPD and a surge-tolerant fuse can provide metallic protection. An alternative method, with GDTs connected in the delta configuration, provides tip-to-ground, ring-to-ground (longitudinal), and tip-to-ring (metallic) protection.

MINIMIZING CAPACITIVE EFFECTS

One of the drawbacks of some solid-state protective devices—TSPDs, for example—is their high, voltage-dependent capacitance, which can cause problems in three areas. Capacitance imbalance due to different biasing voltages on the tip and the ring may cause longitudinal, or common-mode, signal distortion. On-hook/off-hook/ringing transitions can cause sudden transient events to occur on the phone line, possibly changing the capacitance of the channel. Equalization established during modem training becomes suboptimal when the capacitance of the channel shifts. The capacitance of the channel changes instantaneously during the transmission of 30V-p-p signals; these nonlinear channel characteristics may lead to IM (intermodulation) distortion.

The object is to design a protective circuit that will minimize the effects of varying capacitance yet still provide protection compliant with the appropriate regulatory and standards requirements or recommendations.

One method is to use microcapacitance TSPDs, which can have a typical capacitance of 60 pF, or 40% less than a standard TSPD part. When 60 pF is still too much, a good alternative is to put the TSPD in series with a pair of ultrafast-switching diodes in an inverse-parallel arrangement (**Figure 3**). Because the diodes have capacitances of about 10 pF each, the total capacitance across the loop is approximately 15 pF. The fuse is necessary for safety and to guard against power-fault events. Although this approach works well in

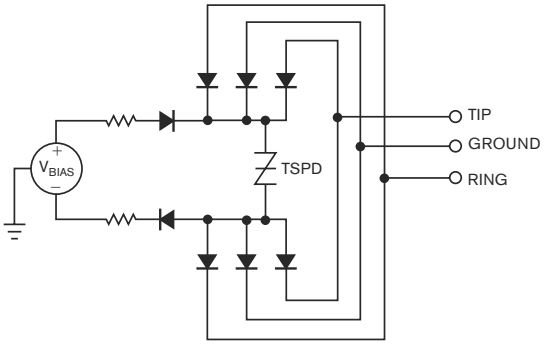

Figure 5 The application of a minimum line bias can reduce and linearize capacitance. A 5V bias applied through two 1-MΩ resistors can serve a circuit with a POTS overlay; a 24V bias works for a circuit without a POTS overlay.

T3 and Ethernet applications, the high peak voltages of VDSL2 (very-high-speed DSL 2) cause the diodes to conduct sufficient current to cause linearity problems that will corrupt the coding constellations.

Figure 4a shows a circuit with two TSPDs that works well for metallic transients on CPE (customer-premises equipment); **Figure 4b** shows a circuit for longitudinal surges on ADSL2+. Another useful circuit is the balanced-bridge topology in **Figure 4c**. Yet another alternative is to apply a minimum line bias to reduce and linearize capacitance. **Figure 5** shows the general topology; a 5V bias applied through two 1-MΩ resistors can serve a circuit with a POTS (plain-old-telephone-service) overlay, and a 24V bias works for a circuit without a POTS overlay.

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For glossaries of overvoltage- and overcurrent-protection devices, go to www.edn.com/ms4307.

Although there are multiple factors to consider when designing protective circuits for DSL, there are multiple useful approaches. Because of the complexities involved, designers may wish to seek advice from suppliers that offer all the circuit-protection technologies and are therefore not biased toward any one type of protective device. EDN

AUTHOR'S BIOGRAPHY

Phillip Havens is telecom-sector technical manager at Littelfuse. He represents the company at many telecom-related industry meetings and helps define, direct, and support new silicon-based protection products. Havens also interfaces with customers' technical teams to develop the most cost-effective protection for their various applications.

NORMAL SIGNALS

Though at times it's unintentional, DSLs (digital-subscriber lines) can experience a number of voltage conditions. One important consideration is whether the loop provides POTS (plain-old-telephone service) as well as DSL. POTS involves battery and ringing voltages. Battery voltage is nominally −48V dc, or 56.6V maximum. Ringing voltage is nominally 90V at 20 Hz in the United States and 25 Hz in Europe, but it can reach 150V rms at 16 to 40 Hz. Therefore, the maximum expected voltage under normal conditions is the peak value of the maximum operating ring voltage, 150V rms, plus the maximum dc bias of the central-office battery, for a total of approximately 269V in the worst-case situation.

HDSLs (high-bit-rate DSLs), on the other hand, use a 1.544-Mbps, T1-equivalent transmission rate but with half the bandwidth of a comparable T1/E1 link. The signaling levels are a maximum of ±2.5V, and loop powering for regenerators is typically less than 190V.

ADSLs (asymmetric DSLs) employ transmission rates that reach 6.144 Mbps from the COT (central-office terminal) to the RT (remote terminal) and as much as 640 kbps from the RT to the COT, whereas VDSL2 (very-high-speed DSL 2) employs symmetrical data rates to 100 Mbps on short loops.

Telephone engineers define overvoltages as metallic (differential mode), between the tip and the ring, or longitudinal (common mode), between the tip and ground or between the ring and ground. Overvoltages can exceed 2500V, and surge currents can reach 500A. Surges can come from nearby lightning strikes or either inductive or direct-contact ac-powerline interactions.

Longitudinal overvoltages are more frequent and are attributable to power induction, power crosses, and nearby lightning strikes, provided that the line is referenced to ground. You can convert one-way longitudinal transients to metallic transients if both the tip and the ring have protective devices to ground and one device conducts before the other.

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Measure power-supply-loop transfer

USING A FUNCTION GENERATOR AND AN OSCILLOSCOPE, YOU CAN MEASURE GAIN AND PHASE SHIFT VERSUS FREQUENCY IN A POWER SUPPLY'S CONTROL LOOP.

Power supplies use control-loop circuits to produce constant voltage or current. The transfer function—gain and phase as a function of frequency—provides valuable information about a control loop's speed and stability. Knowing a control loop's transfer function, as well as the poles and zeros of the transfer circuit, can help you select the right compensation and power-stage components.

You can measure gain and phase shifts and plot them with a network analyzer that sweeps the frequency of an injected signal and automatically computes the control loop's phase difference and gain. Such an instrument is nice to have and convenient—but is also expensive. If you don't have one available, you can make the measurements with an oscilloscope, a signal generator, and a standard transformer.

To perform the measurements, you inject a small ac signal into the power supply's control-loop circuit and measure the loop's gain and phase shift. By measuring the gain and phase, you can plot them with a Bode plot. The gain and phase differences between the injected signal and the control loop's output are the transfer function.

PREPARE THE CIRCUIT

Figure 1 shows a typical step-down switch-mode regulator with the required measurement setup. Start by breaking the loop of the power supply's regulator circuit (highlighted area in **Figure 1**) so you'll have a point at which to inject the small signal and measure the loop's response. You can break the loop at the low-impedance output node above the high-side feedback resistor, R_1, in the feedback path.

You must electrically isolate the measurement points, A and B, by placing a small resistance, such as 20Ω, in the control loop's feedback path. A 20Ω resistor in the control loop has a negligible effect on the power supply's output voltage, V_{OUT}.

To inject the signal into the control loop and make the measurements, you need a sound measurement structure. The online version of this article contains a **sidebar**, "Good connections," that explains how to modify a regulator-IC evaluation board for these measurements (www.edn.com/ms4284).

The injected signal must be small in relation to the output voltage so that it won't change the way the power supply handles large signals. Yet, the injected signal must be large enough that you can recognize it in the control loop. The injected signal must not trigger a voltage-protection threshold at a regulator IC's feedback pin, FB.

You should inject a sine wave with an amplitude of 30 to 100 mV across the 20Ω resistor. The exact signal amplitude you need may change depending on the control loop's gain, and the amplitude will vary with frequency. Start by injecting a small signal and then increase its amplitude as needed until you can see it on an oscilloscope screen. This step ensures that the signal is still small relative to the loop's dc output.

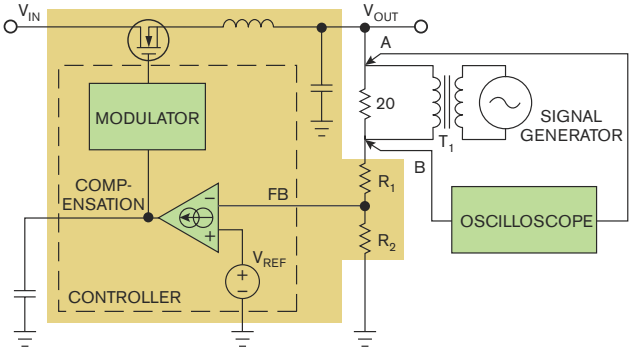

Figure 1 This measurement setup lets you compare an injected sine wave with the signal as it rides on a power supply's output, V_{OUT}.

The injection transformer, T_1, prevents dc from entering the control loop. Look for a transformer that offers a flat voltage transmission over a wide frequency band. If you don't have such a transformer, you can compensate for frequency variations in your transformer's flatness by adjusting the signal generator's output amplitude.

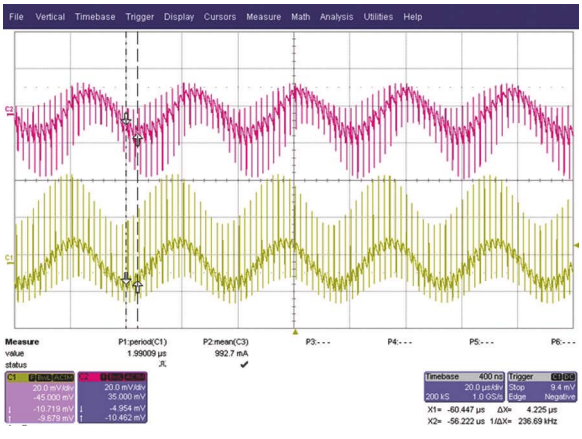

Figure 2 When control-loop gain is 1 (0 dB), the amplitude of the injected signal (upper trace) will equal the amplitude of the output signal (lower trace).

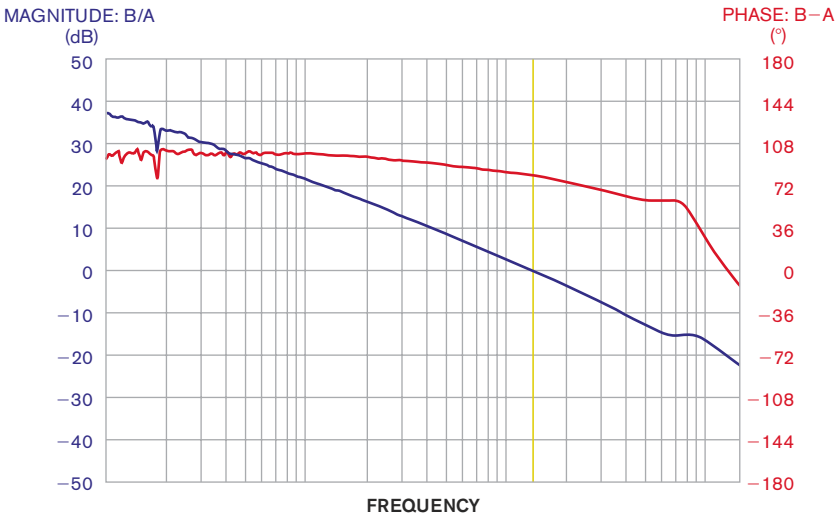

Figure 3 A Bode plot shows the point at which the gain (blue trace) is 0 dB and shows the corresponding phase offset (red trace).

Connect the signal generator to the transformer's primary side, and then turn on the generator. Measure the injected signal across the 20Ω resistor using two calibrated oscilloscope probes. (Attach the ground leads of both probes to a common ground point on the power supply under test.) To make the measurement, you'll need to view the difference between the signals on Channel A and Channel B.

Adjust the signal generator's amplitude so that the transformer's output voltage won't drive the control-loop circuit into nonlinear operation. Set the dc offset of the signal generator's output to 0V because only ac is transferred through the transformer anyway.

To prevent switching noise from filling the oscilloscope's screen and covering the waveform of interest, set the oscilloscope for bandwidth limiting. You can ensure a well-triggered waveform by connecting a third oscilloscope channel to the signal generator's output and triggering on the output signal.

POWER SUPPLY

Next, you should power up the control-loop circuit and make a loop-transfer-function measurement as described above. Repeat this measurement under different load and line conditions. At low output loads, most power supplies will go into discontinuous current-conduction mode, which will change the control loop's characteristics. In voltage-mode control, a power supply's loop characteristics will change with input voltage.

After setting up the equipment and powering the control loop, you should see a line on the channel connected to the output voltage (Probe A in **Figure 1**) and a noisy sine wave on the other channel. If you don't see a sine wave, then set the oscilloscope to the highest-amplitude resolution—typically, 20 mV/division—or increase the amplitude of the signal generator's output.

Once you see a sine wave, change its frequency by adjusting the signal generator. You will see a change in amplitude on Channel A. Look for a frequency in which the sine waves of Channel A and Channel B have equal amplitude; at

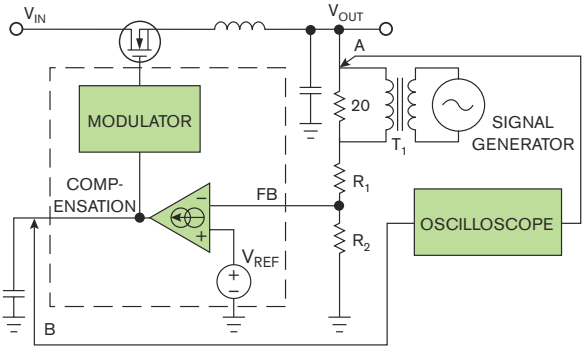

Figure 4 This measurement setup lets you measure the compensation signal of the voltage-regulator IC (Probe B).

Analog Applications Journal

DESIGN BRIEF

Cascading of Input Serializers Boosts Channel Density for Digital Inputs

By Frank Dehmelt
Systems Engineer Analog Products

Introduction

Programmable logic controllers (PLCs) play an integral role in industrial automation. They allow inputs from digital as well as analog sensors and provide outputs to drive actuators. The digital inputs represent a significant share of those I/Os, accepting inputs from end switches, proximity switches, fuel sensors, light barriers, over-temperature sensors and many others.

The Traditional Approach

There are several types of digital inputs; the IEC-61131-2-standard defines those most commonly used. We will first discuss traditional solutions, and then look at a new approach by TI.

Traditionally, digital inputs used discrete components and required a parallel processor interface. Current limitation was achieved by a series of high-power resistors. Resistor-capacitor (RC) filters reduced bouncing of mechanical switches, while a per-channel optocoupler connected to the parallel processor interface. This design, however, requires bulky components, many isolation channels, and a large footprint host controller to allow for the parallel inputs. It also creates significant power dissipation.

With a typical resistor chain providing about 2.2 kΩ, the current at the nominal 24 V rises to 11 mA and results in power consumptions of 260 mW or 400 mW at 30 V. Considering that this dissipation may occur simultaneously for all input channels — along with the bulky components and the processor interface — it severely limits channel density.

A New Approach

TI's SN65HVS88x product family addresses these limitations and more. The digital input serializer (as the name implies) serializes the inputs into a single SPI data stream and reduces the number of isolators by 50%.

The resistors and LEDs shown in Figure 1 are required by the IEC-61131-2-standard; they can be omitted for inputs that do not require conformance with this standard. Regardless, the integrated current limit allows use of a lower power resistor.

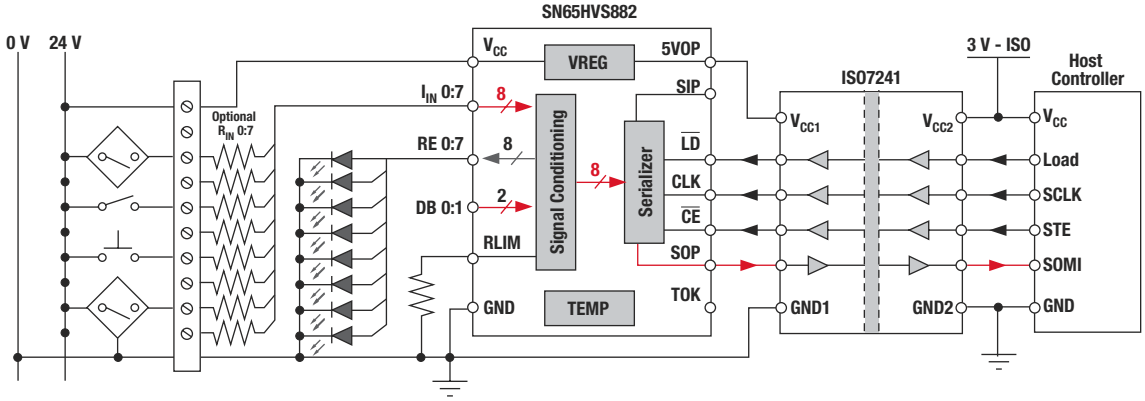

Figure 1. 8-channel digital input using HVS882 and ISO7241

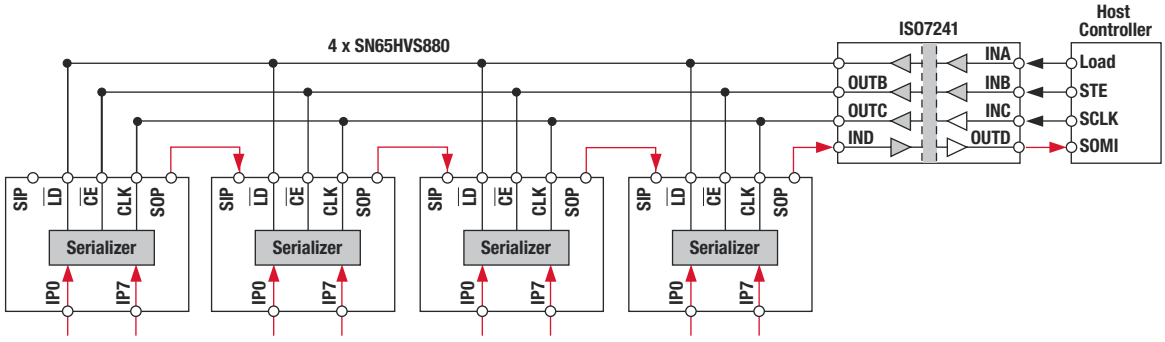

Figure 2. Simplified 32-channel digital input with cascading, using four HVS88x serializers and one ISO7241 digital isolator

The input current is fed to an output pin, which allows it to drive an external LED to indicate the current state of the input. Without the LED, this pin simply connects to ground.

The HVS88x family allows for the cascading of several devices, all sharing the same SPI interface, as shown in Figure 2. For a 32-channel input, it still provides a four-channel isolation, saving 87% of ISO channels.

And what about power dissipation with a 32-channel interface? We previously calculated a worst-case dissipation of 400 mW/channel totaling almost 13 W: this is too much for a PLC slice which is about the size of a deck of cards. The HVS88x family allows the designer to set current limitation anywhere between 200 µA and 5.2 mA. For a type-1 or type-3 switch, choose a limit in the 3-mA range, limiting the per-channel dissipation to 90 mW at 30 V. This reduces power dissipation by more than 75% vs. a discrete approach.

The designer can further reduce the number of external components by using the integrated debounce filter, set to filter pulses of less than 3 ms or 1 ms in duration. For the fastest acquisition of glitch-free switches, bypass the filter as well.

The parts operate from the 24-V nominal field supply and generate the internally used 5 V themselves. This supply is also available to drive external circuitry such as the field side of the isolation barrier on the SPI interface.

The HVS88x family allows high-density digital inputs by serialization, cascading, a significant reduction of power dissipation, and elimination of external components. Production material, samples, and evaluation boards are available. Table 1 presents specifications for the SN65HVS88x devices.

Parameter	SN65HVS880	SN65HVS882
Serialization	Yes	Yes
Cascading	Yes	Yes
Current limitation	Yes (0.2 to 5.2 mA)	Yes (0.2 to 5.2 mA)
Debounce filter	Yes (0 ms, 1 ms, 3 ms)	Yes (0 ms, 1 ms, 3 ms)
V_{CC}	18 V to 30 V	10 V to 34 V
Undervoltage indicator	Yes (~15 V)	No
5-V output	Yes	Yes
Input voltage range	0 V to 30 V	0 V to 34 V
Temperature range	–40°C to 85°C	–40°C to 125°C
Over-temperature protection	Yes	Yes

Table 1. The SN65HVS88x digital input serializer family digital isolator

Reference

1. www.ti.com/sn65hvs882

Related Device

www.ti.com/iso721

For more information, visit:
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this point, the gain of the control loop is 1 (0 dB). This frequency is the loop's 0-dB crossover frequency (**Figure 2**).

Typically, the two sine waves will be phase-shifted relative to each other. The amount of phase difference at the 0-dB crossover frequency is the phase margin of the control loop. Besides measuring the injected and output sine waves at the 0-dB crossover point, you should also measure the sine wave riding on the output voltage at lower frequencies. The amplitude difference between Channel A and Channel B gives the gain at a given frequency. **Table 1** lists the voltage ratio between the injected sine wave and the sine wave riding on the output voltage and the corresponding values in decibels.

You can successfully make these loop measurements on a control loop that doesn't oscillate or is in some sort of hysteretic overvoltage-protection mode. If the error amplifier is a transconductance amplifier, you can achieve a stable loop design by placing a capacitor from the regulator IC's compensation pin to ground. If the error amplifier is a standard voltage-to-voltage error amplifier, then place a capacitor from the compensation pin to the FB pin. A 1-µF capacitor typically works well. It sets a pole at very low frequencies and forces the gain to drop quickly so that the 0-dB crossover is at a very low frequency. In current-mode-control designs, the phase margin at very low frequencies is usually enough to yield a stable circuit.

THE BODE PLOT

To generate a Bode plot, you must sweep the signal generator's frequency across the frequency range of interest and measure the gain and the phase shift between the input signal (Probe B in **Figure 1**) and the output signal (Probe A). For large and small gains, you might have a difficult time seeing results on the oscilloscope screen. At 30-dB gain, for example, it's difficult to see a voltage relationship between Channel A and Channel B.

For typical designs, you can easily and accurately measure the most important points, such as the 0-dB crossover point of a Bode plot. At high gain frequencies, you might have a difficult time viewing the exact decibel value, but you can make a quantitative observation, such as that the gain is probably higher than 30 dB. **Figure 3** shows the control loop's 0-dB-gain crossover frequency, where the blue trace crosses 0 dB.

You can consider loop bandwidth as a combination of the level of dc gain and the frequency of the 0-dB crossover. The control loop's phase-margin measurement can indicate the control loop's stability margin. Depending on the design, you need a minimum phase margin of 45 to 50°. More is better.

Besides using the measurement setup in **Figure 1**, you can connect the oscilloscope channel that was measuring the injected signal (Probe B) to the compensation pin of a power-supply-regulator IC (**Figure 4**). In this setup, you can measure the transfer function of the control loop without the influence of the compensation network (the capacitor that connects to the regulator's compensation pin). With the information you obtain about the power stage with this measurement, you can easily select optimized compensation components for a desired control-loop bandwidth and phase margin. EDN

TABLE 1 COMMON DECIBEL VALUES FOR VOLTAGE RATIOS

Voltage ratio (A/B) (V)	Decibel level (20×log[A/B]) (dB)
0.03162	−30
0.1	−20
0.3162	−10
0.7071	−3
1	0
1.414	3
3.162	10
10	20
31.62	30

The online version of this article contains a link to a seven-minute video that describes the test procedure. Go to www.edn.com/ms4284.

AUTHOR'S BIOGRAPHY

Frederik Dostal is an applications engineer for the power-management group at National Semiconductor.

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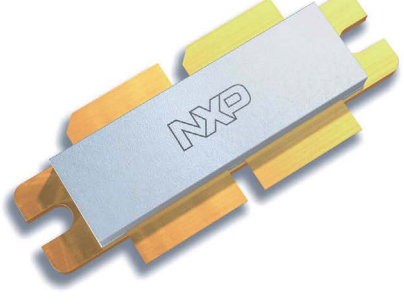
Experience

the power density of bipolar with the benefits of LDMOS



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READERS SOLVE DESIGN PROBLEMS

Solar-array controller needs no multiplier to maximize power

W Stephen Woodward, Chapel Hill, NC

Solar-photovoltaic arrays are among the most efficient, cost-effective, and scalable "green" alternatives to fossil fuels, and researchers are almost daily announcing new advances in photovoltaic technology. But successful application of photovoltaics still depends on strict attention to power-conversion efficiency. **Figure 1** shows one reason for this attention.

A photovoltaic array's delivery of useful power to the load is a sensitive function of load-line voltage, which in turn depends on insolation—that is, sunlight intensity—and array temperature. Operation anywhere on the current/voltage curve except at the optimal maximum-power-point voltage results in lowered efficiency and a waste of valuable energy. Consequently, methods for maximum-power-point tracking are common features in advanced solar-power-management systems because they can boost practical power-usage efficiency—often by 30% or more.

Because of its generality, a popular maximum-power-point-tracking-control algorithm is perturb and observe, which periodically modulates, or perturbs, the load voltage; calculates, or observes, the instantaneous transferred power response; and uses the phase relationship between load modulation and calculated power as feedback to "climb the hill" of the current/voltage curve to the maximum-power-point optimum. The perturb-and-observe algorithm is the basis of the maximum-power-point-tracking-control circuit (**Figure 2**, in yellow) but with a twist (in blue), which achieves a feedback function equivalent to a current-times-voltage power calculation but without the complexity of a conventional multiplier. The idea relies on the well-known logarithmic behavior of transistor junctions, $V_{BE}=(kT/q)\log(I_C/I_S)=(kT/q)[\log(I_C)-\log(I_S)]$, where V_{BE} is the base-to-emitter voltage. It also relies on the fact that adding logarithms is mathematically equivalent to multiplication. Here's how.

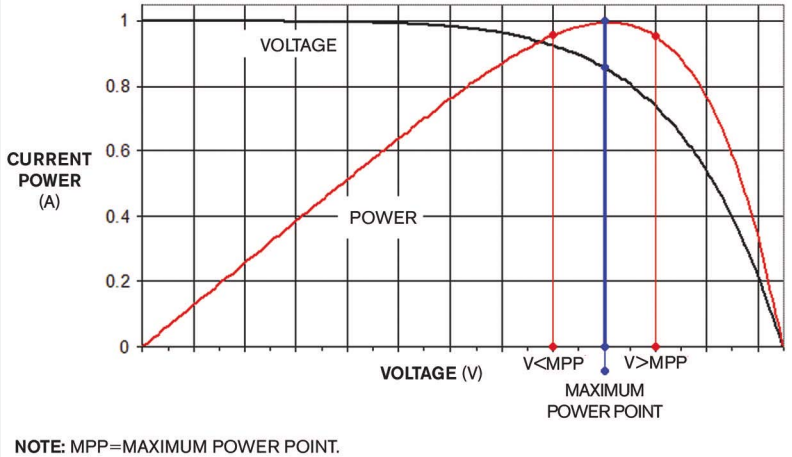

Figure 1 It is important to operate solar-photovoltaic arrays at their maximum power point.

Capacitor C_2 couples a 100-Hz, approximately 1V-p-p-modulation or 1V-p-p-perturbation square wave from the S_2/S_3 CMOS oscillator onto the photovoltaic-input voltage, V. The current/voltage curve of the array causes the input current, I, to reflect the V modulation with a corresponding voltage-times-current input-power modulation. IC_{1A} forces I_{Q1} to equal $I\times x_1$, where I is the solar-array current and x_1 is a gain constant. IC_{1B} forces I_{Q2} to equal V/499 kΩ, where V is the solar-array voltage. Thus, $V_{Q1}=(kT_1/q)1[\log(I)-\log(I_{S1})+\log(x_1)]$, and $V_{Q2}=(kT_2/q)[\log(V)-\log(I_{S2})-\log(499\ k\Omega)]$. V_{Q1} is the base-to-emitter voltage of Q_1; k is the Boltzman constant; T_1 is the temperature of Q_1; q is the elementary charge of the electron; I is the current input

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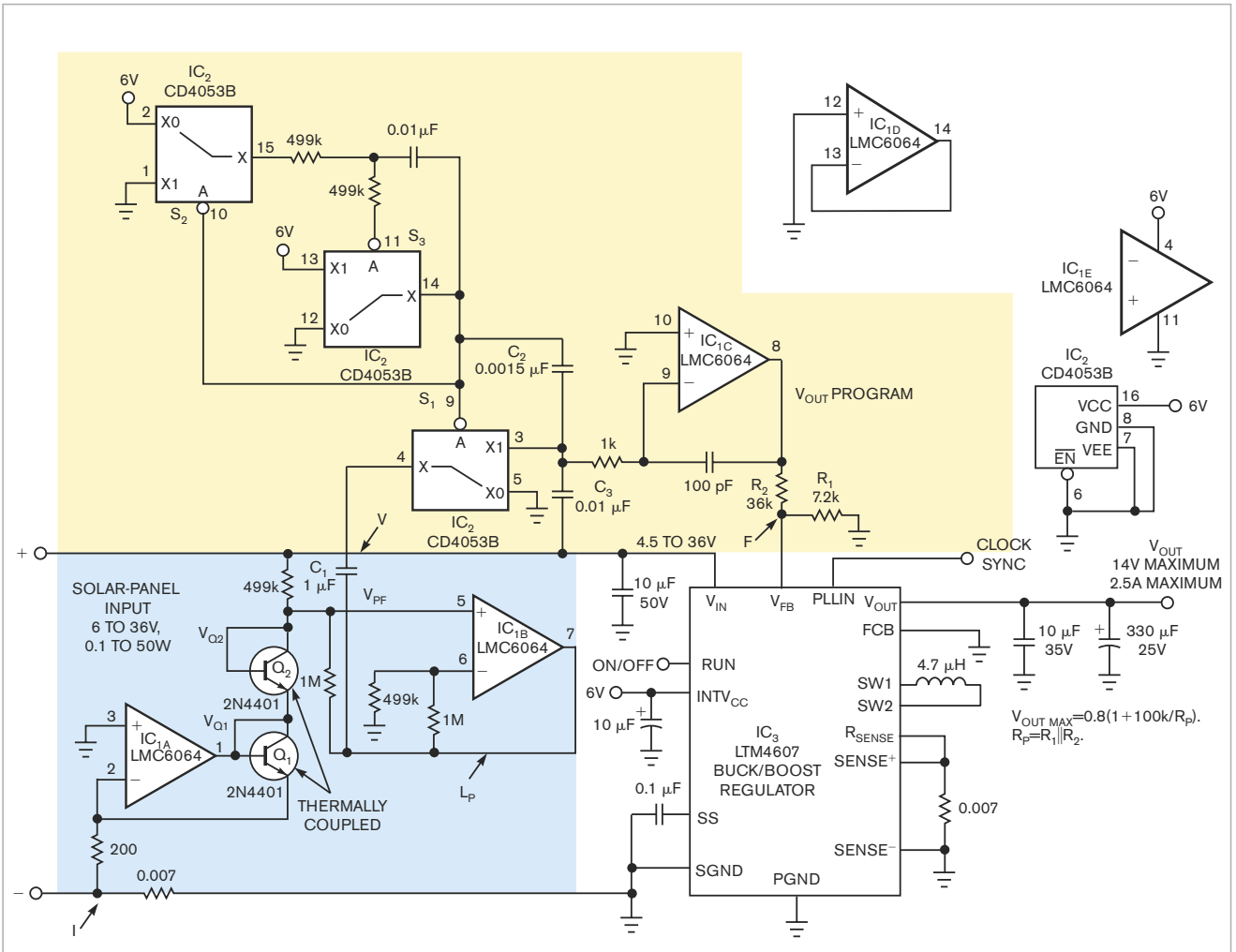

Figure 2 This maximum-power-point-tracking controller relies on the well-known logarithmic behavior of transistor junctions.

from the solar panel's negative terminal; I_{S1} is the saturation current of Q_1; x_1 is the arbitrary gain constant, which IC_3 determines; V is the voltage input from the solar panel's positive terminal; I_{S2} is the saturation current of Q_2; K is degrees Kelvin; V_{PF} is the power-feedback signal; and V_{IP} is the calculated power-input signal. Because k, q, I_{S1}, I_{S2}, x_1, and 499 kΩ are all constants and $T_1=T_2=T$, however, for the purposes of the perturb-and-observe algorithm, which is interested only in observing the variation of current and voltage with perturbation, effectively, $V_{Q1}=(kT/q)\log(I)$, and $V_{Q2}=(kT/q)\log(V)$.

The series connection of Q_1 and Q_2 yields $V_{PF}=V_{Q1}+V_{Q2}=(kT/q)[\log(I)+\log(V)]=(kT/q)\log(VI)$, and, because of IC_{1B}'s noninverting gain of three, $V_{IP}=3(kT/q)\log(V\,I)\simeq 765$ µV/% of change in watts. The V_{IP} log (power) signal couples through C_1 to synchronous demodulator S_1, and error integrator and control op amp IC_{1C} integrates the rectified S_1 output on C_3. The IC_{1C} integrated error signal closes the feedback loop around the IC_3 regulator and results in the desired maximum-power-point-tracking behavior.

Using micropower parts and design techniques holds the total power consumption of the maximum-power-point-tracking circuit to approximately 1 mW, which avoids significantly eroding the efficiency advantage—the point of the circuit in the first place. Meanwhile, simplifying the interface between the maximum-power-point-tracking circuit and the regulator to only three connection nodes—I, V, and F—means that you can easily adapt the universal maximum-power-point-tracking circuit to most switching regulators and controllers. Therefore, this Design Idea offers the efficiency advantages of a maximum-power-point-tracking circuit to small solar-powered systems in which more complex, costly, and power-hungry implementations would be difficult to justify. EDN

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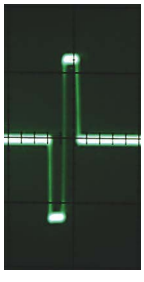

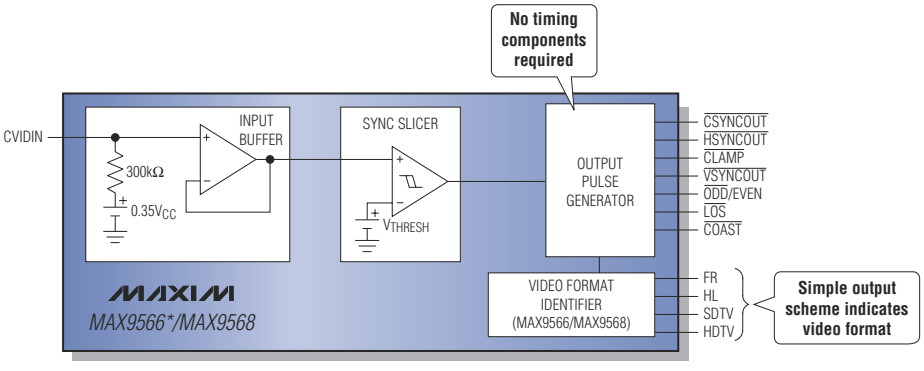

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Simple microcontroller-temperature measurement uses only a diode and a capacitor

Andreas Grün, Wedemark, Germany

Using a PN-junction diode for temperature measurement usually depends on its 2-mV/K temperature coefficient. Conventionally, you must amplify and digitize this voltage with an ADC before you can use the value in a microcontroller. Less well-known is the fact that the *reverse* current of a PN-junction diode shows a good exponential dependency over temperature; increasing the temperature by approximately 12K doubles the leakage (**Figure 1**). An easy way to measure current over such a large range of two to three decades is to charge and discharge a capacitor and measure the time or frequency.

A general-purpose I/O pin of a microcontroller charges a capacitor either by using it temporally as an output or by enabling a pull-up resistor, which is available in some controllers (**Figure 2a**). After charging the pin, you configure it as a high-impedance input, and a capacitor discharges through the leakage current of the diode (**Figure 2b**). The discharge time then is proportional to the temperature of the diode; thus, the diode exhibits exponential behavior. Depending on the type of diode, the exponential behavior can be nearly ideal. Calibration of a base point is necessary because the absolute value of the current varies greatly at a given temperature.

Selecting the diode and the value of the capacitor requires some care. The smaller the PN junction, the smaller the reverse current and the longer the discharging time. Periods longer than a few seconds are usually unsuitable. Making the capacitor's value too low leads to errors because the capacitance of any cable and the capacitance of the PN-junction diode come into effect.

Typically, a power diode, such as a 1N4001 with a capacitance of 1 nF, gives suitable results. The discharge time is approximately 0.3 to 1 sec at room temperature, falling into the millisecond range at 100°C. The PN-junction diode of a power transistor should also work. EDN

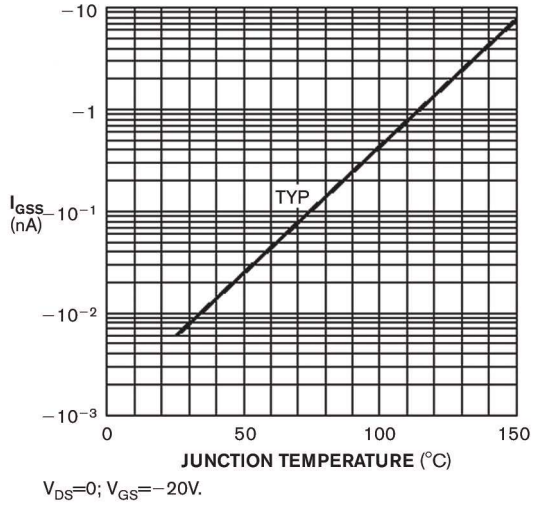

Figure 1 The reverse current of a PN-junction diode shows an exponential dependency over temperature; increasing the temperature by approximately 12K doubles the leakage.

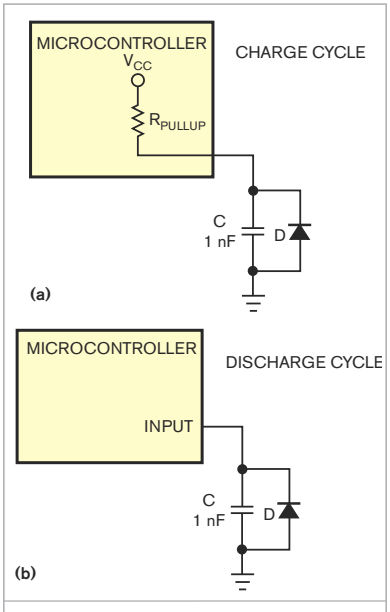

Figure 2 Capacitor C first charges through the pull-up resistance of the microcontroller's I/O pin configured as an output (a). The capacitor then discharges through the reverse leakage of diode D_1 (b).

Current mirror drives multiple LEDs from a low supply voltage

Rex Niven, Forty Trout Electronics, Eltham, Victoria, Australia

Driving LEDs at a regulated current from low supply voltages can be difficult because minimal overhead voltage is available for control circuits. A current-mirror architecture is suitable but usually works only with ICs with well-matched transistors and in which the silicon substrate holds them at one temperature. However, high currents—approximately 100 mA—are not normally possible. A thermal runaway can occur in circuits using unfavorable combinations of discrete bipolar transistors. In this scenario, one LED-driver transistor becomes

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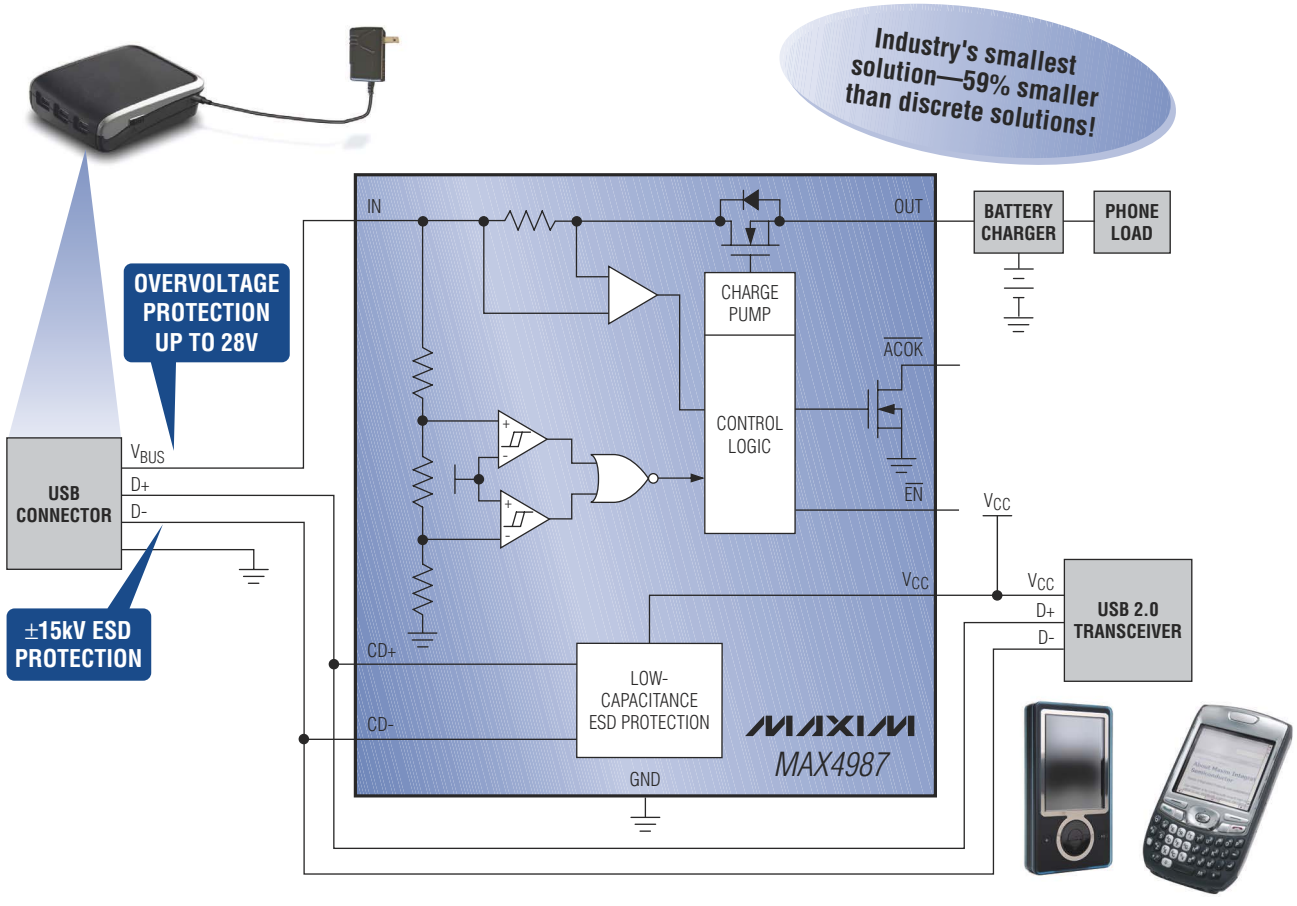

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slightly hotter than the others, its gain increases, and it takes more current and gets even hotter until it self-destructs. This Design Idea shows how you can avoid this problem for pulsed-current-mirror applications.

The current mirror comprises Q_4 through Q_7 with connected bases and emitters, and the collector current of Q_3 is the control output (**Figure 1**). Resistor R_3 converts Q_3's collector current to a feedback voltage. Transistors Q_1 and Q_2 form a voltage-difference amplifier. The control-transistor current after feedback is $1.2V/R_3$, and the LEDs have a similar current. Because of the pulsed operation—say, 25% duty at 3 Hz—the transistor temperature does not reach a stable value and cools again toward the ambient temperature during the off period. The thermal-runaway effect does not have time to develop.

The capacitor prevents transient oscillations at switch-on or -off. Use the same transistor type for Q_4 through Q_7 and mount all of them on the same part of the PCB (printed-circuit board). The supply voltage can be as low as 2.5V for certain LEDs, especially infrared types, and the collector current can exceed 100 mA per LED. EDN

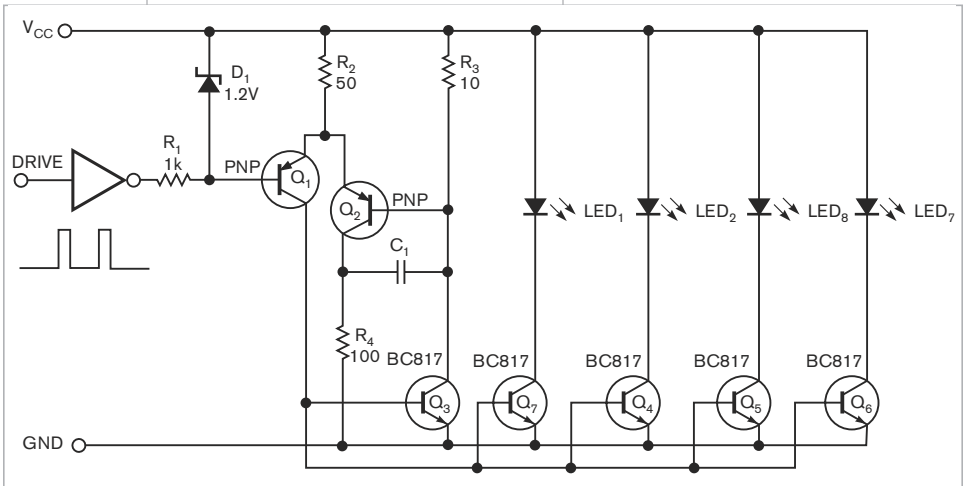

Figure 1 A pulsed-current mirror comprising transistors Q_4 through Q_7 drives multiple LEDs from a low supply voltage.

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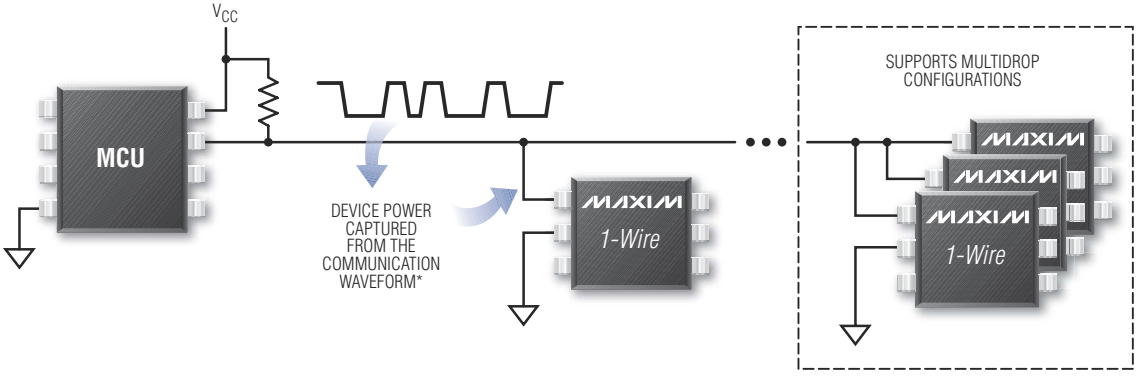

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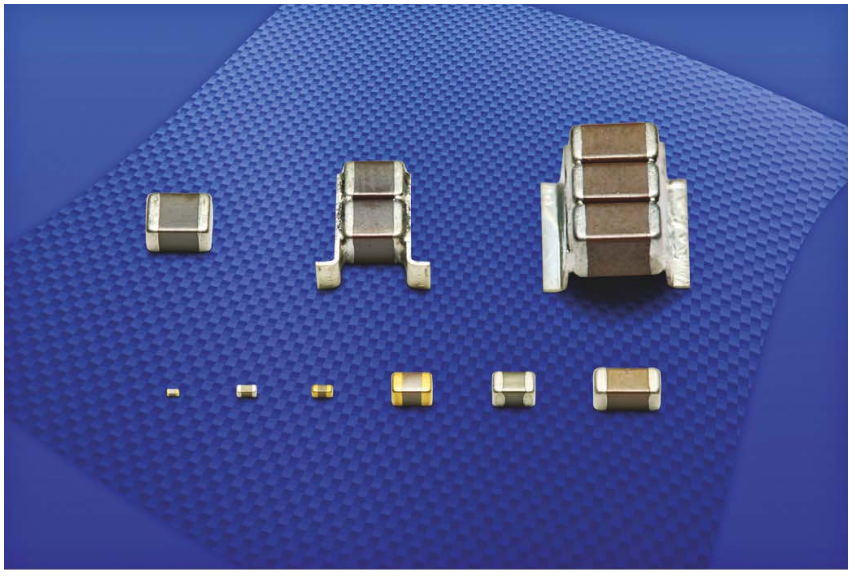

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Aiming at filter applications, the X7R and X5R MLCC (multilayer-ceramic-capacitor) series provides an alternative to polarized-tantalum and electrolytic capacitors. Packaging for the capacitors ranges from 0402 to 1812 case sizes with 100-pF to 100-µF capacitance values. Prices for the X7R and X5R MLCC series range from 1 cent to $1.

Novacap, www.novacap.com

Chip capacitor suits tip-and-ring telecom

Suiting tip-and-ring-telecom applications, the low-profile, MLC chip capacitor features a standard nickel-barrier-solder-plate termination and is compatible with standard surface-mount reflow processes. Aiming at PCMCIA cards with low-profile chips, the capacitor has an X7R dielectric rating of −55 to +125°C with a 1.2-µF capacitance. Features include a 250V dc telco rating and a 625V dielectric withstanding voltage. Available in EIA sizes ranging from 0805 to 2225 with a 0.08-in. maximum thickness, the MLC chip capacitor costs 15 cents (10,000).

AVX Corp, www.avx.com

Thick-film chip resistors offer high resistance values

Using the fine-line patterning of the vendor's HVC series, the precision thick-film HGC chip-resistor series provides high resistance values in voltage dividers for test instruments, meters, and monitoring equipment; voltage-regulation modules; and circuitry. The resistor uses a proprietary method of depositing the thick-film-resistance material on the ceramic substrate. The process yields a stable resistance element, allowing noise reduction and providing a wider range of resistance values than do other high-resistance-value chip resistors. The vendor's deposition method allows for the reduction of ohms per square inks, achieving higher resistance values; lower ohmic-value inks are inherently more stable than those with higher ohmic values. The series is available in 0402 to 2512 sizes, 1-kΩ to 2-TΩ resistance, 0.25 to 20% tolerances, and 25- to 200-ppm TCRs. Prices depend on size, tolerance, TCR, and resistance value and range from 50 cents to $4.

Stackpole Electronics, www.seielect.com

Chip resistor doubles maximum voltage rating

Requiring minimal PCB (printed-circuit-board) space, the 3W-rated SC-3 series chip resistor comes in a 1W, 1225 chip size. Features include a 1Ω to 100-kΩ resistance range, a maximum voltage-ratings increase from 50 to 100V, and 3W power dissipation at 70°C. The resistive component suits inrush-current limiting in power supplies, current-setting resistors in constant-voltage LED circuits, and applications requiring low-profile resistors. The device supports a ±1% absolute tolerance with TCRs of ±100 ppm/°C and a −55 to +150°C operating temperature. The SC-3 chip-resistor series costs 30 cents (10,000).

International Resistive Co, www.irctt.com

Z-Foil resistor claims near-instantaneous thermal stabilization

Using the vendor's Z-Foil technology, the VPR221Z ultrahigh-precision resistor claims a 1-nsec ther-

PASSIVES

mal-stabilization rise time without ringing; other resistors take several seconds. The device provides an industrial-grade ±0.05 TCR ppm/°C from 0 to 60°C and ±0.2 TCR ppm/°C from −55 to +125°C, with a 25°C reference and an 8W power rating at 25°C in accordance with the MIL-PRF-39009 standard. The resistor also provides a ±4 ppm/W typical power coefficient and a ±0.01 tolerance. The device withstands 25 kV of electrostatic discharge and provides 0.5 to 550Ω resistance values. The vendor can manufacture it to meet resistance values in the given resistance range without altering the cost of lead-time. The VPR221Z precision Z-Foil resistor costs $7.

Vishay Intertechnology, www.vishay.com

COMPUTERS AND PERIPHERALS

Notebook memory provides low-latency profiles

The ultralow-latency, 800-MHz DDR2 HyperX notebook memory comes in 4-Gbyte memory kits. The SO-DIMMS come in two preprogrammed profiles at 1.8V: the DDR2-800 CL4-4-4-12 and the DDR2-667 CL3-4-4-10. The HyperX PC2-6400 CL4 notebook memory SO-DIMMs kit of two costs $257.

Kingston Technology, www.kingston.com

Graphics cards feature 320 stream-processing cores

Supporting DirectX 10.1 games, the ATI Radeon HD 4650 and HD 4670 graphics cards use the vendor's TeraScale graphics engine with 320 stream-processing cores. The 4650 operates at less than 50W at full load; the 4670 operates at less than 60W at full load. Available with a frame buffer of 512-Mbyte GDDR2 memory, the 4650 costs $69; the 4670 comes with a frame buffer of 512-Mbyte GDDR3 memory and costs $79. A 1-Gbyte DDR3-based variant is also available.

AMD, www.amd.com

Wide-screen LCD touts four-way ergonomic capability

The MultiSync EA221WM 22-in. wide-screen LCD allows simultaneous side-by-side application windows. Features include 5-msec response time, a 176° viewing angle, a 1000-to-1 contrast ratio, and 1680×1050-pixel WSXGA resolution. The device provides four-way ergonomic capability, including height, swivel, tilt, and pivot/

COMPUTERS AND PERIPHERALS

portrait; a four-port USB hub; and built-in multimedia speakers. The LCD also includes 250 cd/m² brightness and HDCP (high-definition copy protocol) over DVI (digital-visual interface). The MultiSync EA221WM widescreen display costs $389.99.
NEC Display Solutions,
www.necdisplay.com

INTEGRATED CIRCUITS

Automotive-grade cross-point switch complies with AEC-Q100

The automotive-grade DS25CP102Q LVDS (low-voltage-differential-signaling) cross-point switch suits infotainment, instrument-cluster displays, GPS navigation, and back-up- and lane-departure-camera-warning systems. Consuming 105 mW power per channel, the 2×2 cross-point switch meets AEC-Q100-standard-certification requirements. Operating at temperatures as high as 85°C, the switch provides 3.125-Gbps data-transmission rates and features selectable transmitter pre-emphasis and receiver equalization. Available in an LLP-16 package, the DS25CP102Q LVDS cross-point switch costs $6.54 (1000). An evaluation board is also available.
National Semiconductor,
www.national.com

RF-receiver chip aims at 300- to 930-MHz frequency bands

Targeting use in the unlicensed-ISM (industrial/scientific/medical) and SRD (short-range-device), 300- to 930-MHz frequency bands, the highly integrated MLX71122 frequency-agile RF-receiver chip has a programmable PLL. The multichannel receiver IC allows large frequency jumps across regional bands, such as the US 315- and 915-MHz and Euro-

pean 433-MHz bands, without changing the RF hardware. Requiring no external ceramic-filter or discriminator components, the chip includes an internal IF filter and FSK/ASK (frequency-shift-keying/amplitude-shift-keying) demodulators. The device accepts a 3 to 5.5V supply voltage with typical 11-mA current consumption and has 50-nA current draw in standby mode. The receiver input sensitivity is as low as −112 dBm for ASK and −107 dBm for FSK signals. Additional applications for the receiver IC include automotive-remote-keyless entry, tire-pressure-monitoring systems, security systems, home automation, garage-door openers, wireless door bells, baby monitors, and wireless headsets. Available in a 5×5-mm lead QFN-32 with a −40 to +105°C temperature range, the MLX71122 costs $1.67 (100,000).

Melexis, www.melexis.com

Image-signal processor has dual-camera support

The STV0986 advanced image-signal processor includes dual-camera support, suiting mobile-imaging applications. The processor supports camera modules including SMIA (standard-mobile-imaging-architecture)-compatible sensors with 5M-pixel resolution. A twin-video-processing-pipeline architecture enables a reduced shutter-delay time. The STV0986 mobile-imaging processor costs $4.

STMicroelectronics, www.st.com

Audio DAC integrates speaker and headphone amplifiers

Integrating speaker and headphone amplifiers, the 24-bit AK4373 stereo DAC eliminates the need for large capacitors for ac coupling. The headphone amplifier operates in differential or single-ended mode and provides output power of 90 mW into 8Ω. The mono-bridge-tied-load speaker amplifier drives 800 mW into 8Ω. The device consumes 7 mW in playback mode. DSP functions include highpass and lowpass filters, stereo separation, five-band equalization, and automatic level control. Features include a power-supply-management function, allowing block-by-block control of circuits, using a three-wire or an I²C microcontroller interface for control. The operating-voltage ranges from 2.2 to 3.6V in analog cores, 2.2 to 4V for the headphone/speaker amplifier, and 1.6 to 3.6V for digital interfaces. Available in a 5×5-mm QFN-33 package, the AK4373 stereo DAC costs $1.14 (10,000).

AKM Semiconductor, www.akm.com

"Long, dark season" for OEMs, Gartner predicts

The holiday season is shaping up to be less than jolly for many members of the electronics supply chain. Bucking the usual trends, several OEMs (original-equipment manufacturers) in the late third and early fourth quarters stated decisions not to increase production of electronic equipment for the holiday season, in anticipation of weaker demand from consumers as the global economic crisis continues.

According to Gartner Inc (www.gartner.com), such action causes "extreme variations in the electronic-systems supply chain"—from ODMs (original-design manufacturers) and EMS (electronic-manufacturing-services) companies to chip-packaging and chip-foundry companies—and the result will be reduced

fourth-quarter orders for chip vendors.

"Because of the manufacturing leadtimes, wafer manufacturers have only recently reduced wafer builds significantly. As a result, many wafers manufactured in the third quarter will sit as inventory in the fourth quarter. Moreover, wafer-infusion starts in the fourth quarter and the first quarter of 2009 will be significantly reduced because fabs will be stuck with inventory manufactured before the financial crash. The speed and intensity of these knock-on effects suggest that the supply chain is planning for reduced demand well into the first quarter of 2009," Gartner analysts Andrew Phillips (**photo**) and Jim Walker wrote in a report.

"Gartner's anecdotal evidence from the Asia/Pacific region and Japan supports the trend for a weak fourth quarter in the semiconductor-supply chain, as they account for two-thirds of semiconductor sales worldwide," the analysts said.

Gartner expects the greatest impact to be on high-end consumer electronics, such as laptops, LCD TVs, media players, and portable navigation devices. The impact on 3G (third-generation) mobile phones should be less because contract renewals with operators, in which a handset upgrade is obligatory, often determine demand.

GREEN UPDATE

IPC FIRED UP ABOUT POSSIBLE TBBPA ROHS INCLUSION

The IPC (www.ipc.org) has voiced concern over the possible inclusion of TBBPA (tetrabromobisphenol A) in the coming revised EU ROHS (European Union restriction-of-hazardous-substances) regulations. As of mid-October, TBBPA, a reactive component for producing flame-retardant epoxy systems and a component in most PCB (printed-circuit-board) laminates, was on a draft list of five substances for priority examination under ROHS.

"TBBPA has already undergone a comprehensive EU risk assessment and, therefore, is not expected to be subject to authorization under REACH [registration, evaluation, and authorization of chemicals]," says IPC President Denny McGuirk.

REACH entered into force on June 1, 2007, to streamline and improve the former legislative framework for chemicals in the European Union.

"The recommendation for priority review of TBBPA under ROHS seemingly undermines the EU's emerging chemicals policy and law under REACH. We urge the [European] Commission to reconsider the inclusion of TBBPA in its list of priority review substances under ROHS," McGuirk says.

According to the IPC, more than two-thirds of the world's electrical and electronic appliances use TBBPA. A ban on TBBPA would have a tremendous impact on the electronics industry in Europe, the industry group believes.

OUTLOOK

NAND OVERSUPPLY COULD AFFECT OTHER INDUSTRIES

NAND sales, which consumer products mainly drive, now face crumbling consumer confidence arising from poor global economic conditions. With the challenging retail situation and the inventory overhang among OEM (original-equipment-manufacturer) customers, NAND-chip suppliers have cut chip prices to increase their sales, iSuppli Corp (www.isuppli.com) says.

According to iSuppli estimates, unit shipments of 1-Gbyte-equivalent NAND chips will likely rise by 126% in 2008, down from 179% in 2007 but still representing tremendous unit growth. That growth, however, has resulted in oversupply. In 2009, unit growth will decline to 71%, iSuppli projects, noting that, over the past five years, the market has averaged a 192% annual increase.

On the oversupply, analysts expect ASPs (average selling prices) of 1-Gbyte-equivalent NAND chips to drop by 62% in 2008, followed by a 50% decline in 2009.

Decreasing unit growth in the NAND-flash market potentially will affect the semiconductor-capital-equipment industry as NAND-flash suppliers have been increasing their capital spending to increase their capacities. Analysts expect industry spending to decrease by 38% in 2009, according to the company's data.

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BY JIM DELMONICO • GENERAL ELECTRIC

All analog, all the time

DANIEL VASCONCELLOS

I was a rookie engineer fresh out of college in the late '80s. I had enjoyed long hours building analog-electronic projects as a hobby and thought that the digital world would be so much easier than analog electronics. After all, computer signals were all ones and zeros.

My first assignment was to write diagnostic software for a new RISC workstation. I relished the freedom from pesky analog signals as I rolled out diagnostic programs for the system. The project's hardware guru designed the SDRAM-interface ASIC and helped out with an optional cache-RAM module. He assigned me the cache-RAM diagnostic.

I did my best to write a bulletproof diagnostic. The optional cache-RAM module attached to the motherboard in a piggyback style using four dense, low-profile, high-speed connectors. The module's designer had allocated a good number of the connector pins to ground and power to feed the power-hungry synchronous-static-RAM chips. The diagnostic found all manufacturing-yield problems, and I was proud of myself.

Soon, though, some systems with the cache-RAM modules installed would fail intermittently when the system was running a real operating system. These infrequent failures were impossible to track down with a logic analyzer because the cache's 128-bit-wide data bus had 24 bits of address and several clocks. I didn't have the equipment to instrument that much cache capacity.

I humbly requested advice from the guru. He asked whether I had looked at any of the signals with an oscilloscope. Then, he smiled and led me to the lab. He probed a few data and address lines at the CPU and cache RAMs and left the scope on infinite-persistence mode as he booted the system several times. He showed me some odd outliers in the scope's eye patterns. Then, he told me to repeat the boot but to hold one scope probe on any cache RAM's ground pin.

The ground potential on the cache module intermittently differed from ground on the motherboard. He then lectured me on how everything, even digital circuitry, is analog.

He instructed me to add a diagnostic test that alternated writing and then reading back all ones and all zeros to sequential cache locations.

A significant amount of current was alternately flowing into the cache module from the power supply when the data bus was charging to logic one and then returning through ground when discharging the data bus to logic zero. The cache RAM's drivers were exhausting the local power-decoupling capacitance on the cache-RAM module when charging the wide cache-data bus. In addition, the ground path between the cache module and the motherboard had too much impedance to handle the current flow between the boards. This situation intermittently caused the logic levels at the CPU to miss the specified voltage specification for logic low, logic high, or both, causing data corruption.

The guru said that the module suffered from ground bounce. I was dumbfounded. He added more decoupling and bulk capacitance to the cache module and directed the designer to add a dedicated ground plane on the cache-RAM module's PCB (printed-circuit board) to reduce ground impedance. These changes fixed the problem.

I learned a lot on that day and have had the opportunity to give the same lesson to many young engineers, who were equally shocked when they, too, learned that everything is analog. EDN

Jim Delmonico is an engineer at General Electric (Skaneateles, NY). You can reach him at jim.delmonico@ge.com.

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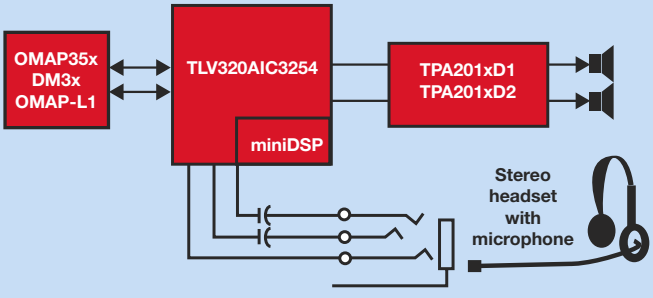

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